An FPGA Can Control Its Own Reconfiguration

An XC4000 or XC5200 FPGA can initiate its own reconfiguration by driving its own PROGRAM input Low. This is a reliable operation although the reconfiguration sequence stops the output from driving PROGRAM Low; the reconfiguration process, once triggered, will continue.

For example, an FPGA could have multiple configurations stored in a parallel PROM, selected by a binary switch that drives the upper PROM address lines. The FPGA could also use these codes as input, comparing them against an internal code that is uniquely determined by the configuration. When you turn the switch, the mismatch is detected and a new reconfiguration is initiated, according to the new switch setting. The reconfiguration could also be delayed until additional conditions are met.

Even without a manually operated switch, the FPGA can initiate reconfiguration to a selected section of the parallel PROM if an external CMOS latch or register is used to maintain the most significant bit(s) of the new PROM address throughout the configuration process.

If you have any novel FPGA or CPLD applications that you would like to share with other readers, send them to editor@xilinx.com. ◆