XC4300 HardWire™ Array Design Verification Form

Company Name _____ Date _____

Customer Name _____ E-mail _____

Address _____ City _____ State/Province _____

Country _____ Zip _____ Tel ( ) _____ Fax ( ) _____

Customer Internal Part Number _____

FPGA File Name and Revision Date _____

Xilinx HardWire Array Device # _____ Temp. Grade (Check One) ☐ C ☐ I

(see cross reference table in HardWire Data Book for correct part number)

Package _____

HardWire Mask Options: (see XC4300 Mask Options in the HardWire Data Book for more information)

Configuration Emulation:

Instant ON ☐ Power On Reset Time: ☐ Short ☐ Long Startup Clock: ☐ CCLK ☐ User CLK

Data Swallowing ☐ Configuration Rate: ☐ Fast ☐ Slow

Sync-To-Done ☐

Start-up Timing: Done Active _____ Outputs Active _____ GSR Inactive _____

Internal Resistor Options:

☐ Done Pull Up ☐ M1 Pull Up ☐ TDO Pull Up

☐ M1 Pull Down ☐ TDO Pull Down

Boundary Scan Enabled? ☐ Always ☐ Only prior to configuration ☐ Never

Customer Special Options:

Special Processing Requirements ☐ Yes ☐ No Customer Specification # _____

(Tape and Reel, Special Packaging, etc.)

☐ Custom Marking Form Attached ☐ Standard Xilinx Marking

Customer Part Marking for Device Package (Optional - 11 Characters max.) ☐☐☐☐☐☐☐☐☐☐☐

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed Design File and the revision date is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire fabrication process.

Customer Name _____ Signature _____ Date _____

For Xilinx Use Only

Xilinx HardWire Design Center Manager: _____ Signature _____ Date _____

Xilinx Customer Service: _____ Signature _____ Date _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date _____

Xilinx Part Number (HPC Code): _____

Mask Set _____ Hole Mask _____ Program Code _____