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FPGA Design Cycle Time *Reduction and Optimization*

With the availability of high-density FPGAs (XC40250XV, 500K system gates) design implementation and verification are performed in parallel to meet time-to-market requirements. You are often forced to make functional changes to your design during the synthesis and implementation phase. These changes commonly termed as "Engineering Change Orders" (ECO) need to be implemented with minimal impact to the netlist, to preserve the original layout. For minor RTL changes, the traditional top-down iterative design methodology requires time consuming re-synthesis and re-layout for the complete design.

At Marconi S.p.A., the designers have developed a top-down/bottom-up synthesis methodology to accommodate ECOs, eliminating the need for complete design re-synthesis and re-layout. This methodology preserves netlist names of all current parts not affected by RTL functional changes enabling the design to use guided place and route. This methodology works with Synopsys FPGA and Design Compilers and requires in-depth knowledge of dc_shell, the Synopsys scripting language.

TRADITIONAL TOP-DOWN DESIGN METHODOLOGY

The traditional FPGA design cycle represented in **Figure 1** requires you to complete the RTL before entering the synthesis and layout cycle.

Using this approach, every small change in RTL necessitates repeating the synthesis and place and route stages of the complete design because synthesis does not preserve the netlist names. As a result, design iterations are very time-consuming and synthesis and layout can become the significant part of the design cycle. This design strategy is quite simple but has its challenges:

- Start of the synthesis phase constrained to the end of the RTL description
- Large amount of memory required for the synthesis process for large designs (above 50K gates)
- CPU time increase for synthesis and layout iterations
- RTL changes imply new synthesis and layout iterations
- No layout reuse capability

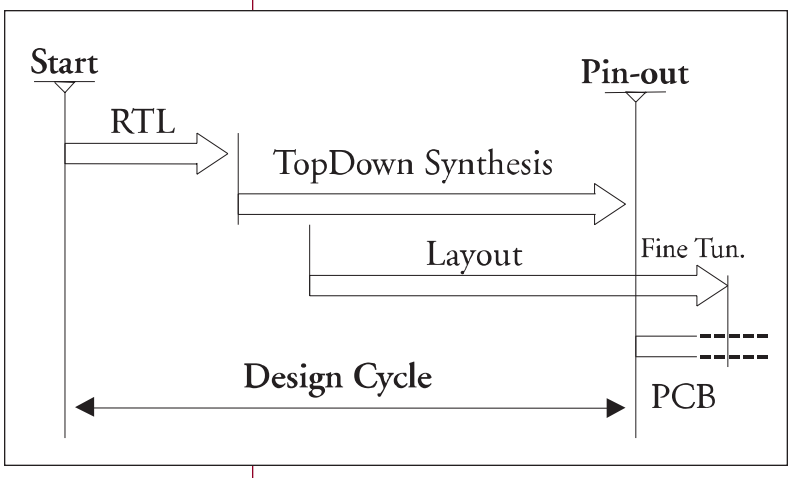

Figure 1

> *"...the designers have developed a top-down/bottom-up synthesis methodology to accommodate ECOs, eliminating the need for complete design re-synthesis and re-layout."*

Due to the limitations using the traditional top-down design methodology and intense time-to-market requirements, the engineers at Marconi have developed a methodology that reduces the design cycle (as shown in **Figure 2**) using Top-Down/Bottom-Up synthesis, and post-layout synthesis capability (layout reuse).

Top-Down/Bottom-Up synthesis capability

This synthesis strategy is commonly used in an ASIC design flow. The hierarchical levels in the design are synthesized individually, then merged at the top-level. The complete design is then placed and routed using the Xilinx Alliance Series implementation tools. It leads to a tradeoff between process memory allocation and design constraints management.

The procedure is simply managed by setting, in a dedicated file, some mandatory variables such as the synthesis session name, the RTL file names, and the top-level module name. Once the design has been completely synthesized, the first layout iteration can take place.

Post-layout synthesis capability

After completion of the first design iteration, a post-layout synthesis algorithm (dc_shell script) is used to preserve netlist names during re-synthesis in all circuit parts not affected by the RTL functional change. This post layout synthesis capability is also called ECO capability. Since this methodology is very efficient for small design changes, highly partitioned designs and good partitioning RTL rules are essential for efficiency.

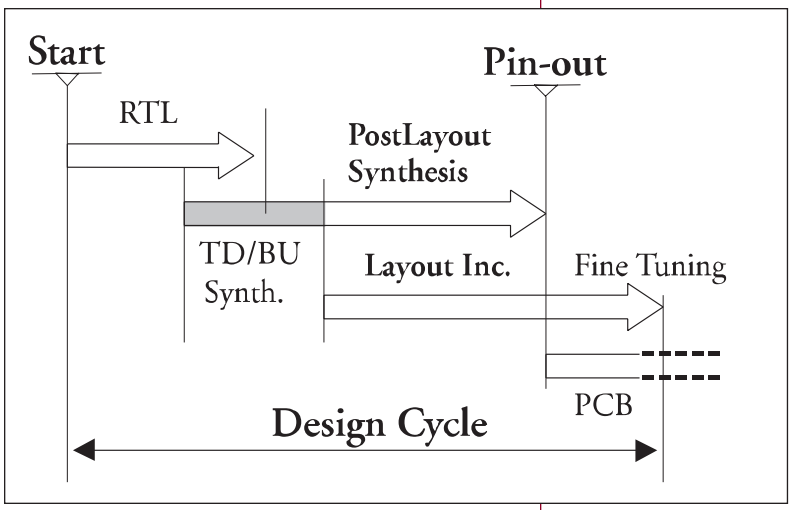

Figure 2

This ECO synthesis methodology, working in conjunction with a guide file, may reduce the design runtimes up to 10x.

Conclusion

Because FPGA densities are increasing rapidly, ASIC design methodologies are now suitable. The ASIC flow proposed here can reduce your FPGA design cycle time by means of advanced synthesis and layout techniques allowing you to control the design development at every phase, avoiding the limitations imposed by the standard synthesis techniques. In the future, with the availability of one million gate FPGAs (the Virtex family of devices) formal verification algorithms will be essential to further reduce the design cycle time for ECOs.

The dc_shells used for the Marconi design methodology may be obtained by contacting your local Xilinx FAE. ◆