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HDL VERIFICATION SPECIAL SECTION

by Troy Scott, Technical Product Manager, OrCAD Express

Board Design and Simulation Using OrCAD Express

OrCAD Express complements the Xilinx Alliance Series and Foundation Series software by providing robust system-level design capabilities. Because a majority of electronic design engineers who develop programmable logic are also responsible for the system-level documentation (such as schematics, bill of materials for production, and a PCB layout netlist), OrCAD set out to ensure that, with OrCAD Express, it would be easy to verify and integrate Xilinx CPLDs and FPGAs into the system. The typical workflow for one or more progammable devices adjacent to the system design workflow is illustrated in **Figure 1**.

Device Design and Simulation

OrCAD Express includes Xilinx Unified Libraries and a LogiBLOX interface for schematic design, VHDL models for functional and timing simulation, as well as RT-level synthesis which provides a solution for a majority of the programmable logic design flows.

All Xilinx CPLDs and FPGAs can be debugged and confirmed with the behavioral and gate-level simulation of OrCAD Express. Schematic debugging is eased with schematic cross-probing and signal-state annotations on the schematic, as well as the necessary VHDL debugging facilities to confirm that models operate correctly before synthesis.

Auto Symbol Generation

To help document large I/O count devices at the system level, many engineering groups create electrical symbols of the FPGA using a pin naming convention based on the names used in the design. **Figure 2**. illustrates a typical signal-to-package-pin name transition. **Figure 3** shows the electrical symbol created by the Generate Part tool of Express.

Step 1 locks a signal to a specific package pin with schematic properties (as in the LogiBLOX pad symbol) or as a VHDL signal attribute of RT-level source. Step 2 uses Xilinx Alliance Series software to implement the CPLD or FPGA and create a signal/pin map file. Step 3 illustrates the electrical symbol of the FPGA that will appear on the system schematic for production and PCB layout. Pins programmed by NGDBuild appear here on the electrical symbol.

Board Design with Express CIS

OrCAD Express includes thousands of symbols for system-level design and, when used in conjunction with the Component Information System (CIS) option, ensures that correct and complete data about the Xilinx FPGA or CPLD is available for production of the system. **Figure 4** illustrates the part data base explorer which adds important parametric data to the basic electrical FPGA or

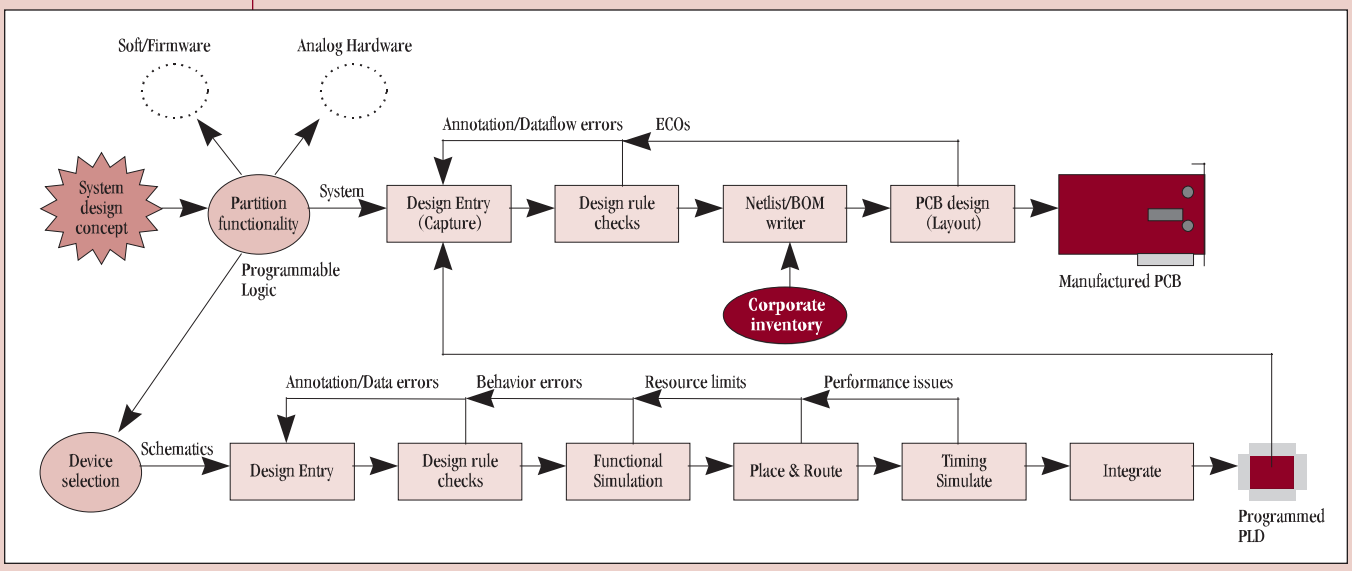

Figure 1. Programmable logic in the system design workflow.

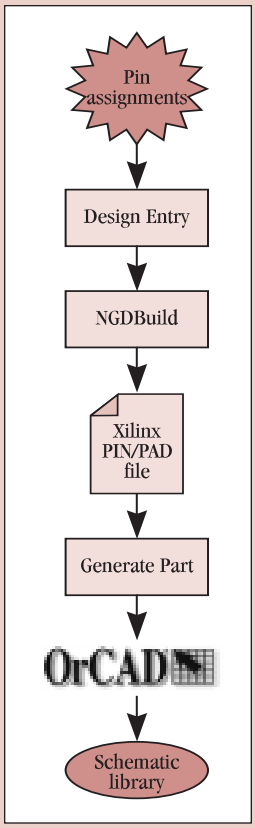

Figure 2. Pin constraints to schematic symbol flow.

CPLD symbol. Properties such as PCB footprint, and corporate inventory part number, that are crucial for the engineering hand-off to production, are transferred to the schematic or merged with the bill of materials.

Simulating Multiple Devices

To confirm the operation of multiple devices created by the Xilinx Alliance Series or Foundation Series software, Express allows you to model the gate-level netlists and VHDL model descriptions of the CPLD or FPGA. Other digital components of the system schematic such as memory or bus interfaces can be modeled with VHDL bus-functional models to verify system behavior.

Simulating a Board Using VHDL Models

Express allows the use of RT-level VHDL models for synthesis as well as a general modeling language for system-level simulation. The Express schematic system makes it easy to get started with automatic model template generation. **Figure 5** illustrates the steps to quickly create a VHDL model template from a symbol on the system schematic.

For more information on Orcad Express, visit www.orcad.com.

Author biography

Troy Scott is the Technical Product Manager for OrCAD Express at OrCAD (Beaverton, Ore.). He received his BSCE degree with Technical Communication Option from the Oregon Institute of Technology (Klamath Falls, Ore.). During his six years at OrCAD, Scott has worked in technical services, documentation, testing, marketing, and software engineering. His current interest is high-level design methodologies for programmable logic using EDA technology. ◆

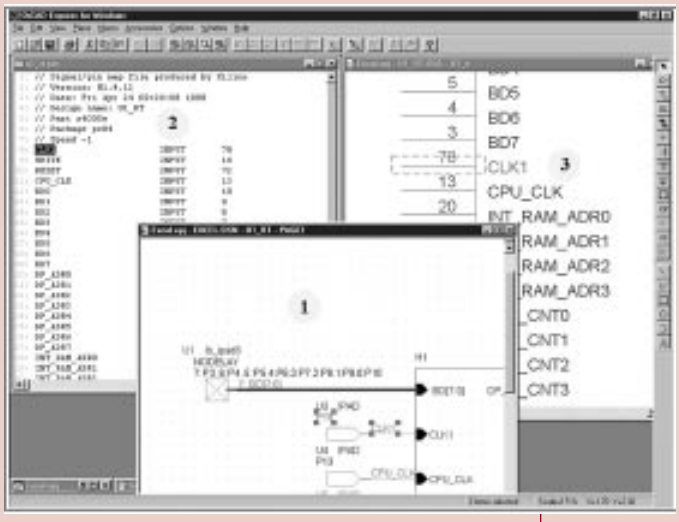

Figure 3. Xilinx pin (PLOC) constraints to symbol generation in OrCAD Express.

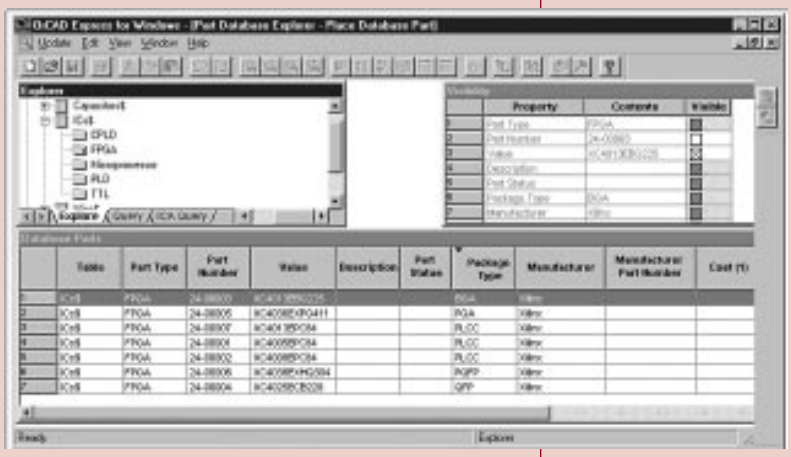

Figure 4. Express CIS part database explorer.

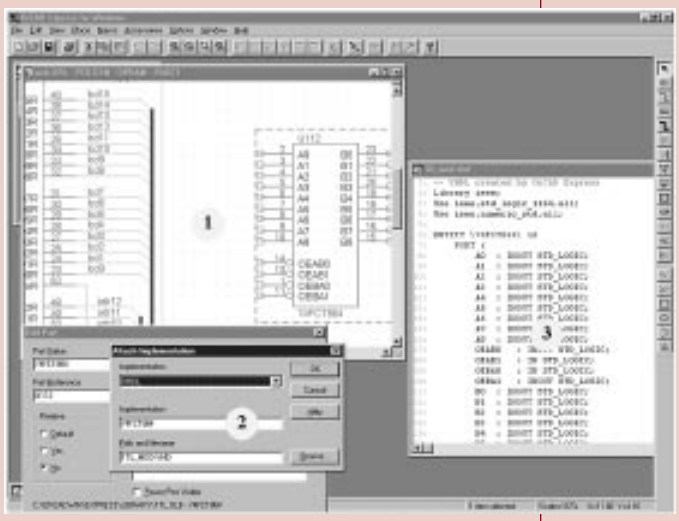

Figure 5. OrCAD Express generates VHDL model template from the schematic editor.