



XC4000E Select-RAM™ Memory: Flexibility with Speed

XBRF 001 April 28, 1997 (Version 2.0)

Application Brief

Summary

The Xilinx XC4000 Select-RAM memory offers the best size flexibility and at the same time offers high speed operation with very little waste.

Xilinx Family

XC4000E/EX

Introduction

FPGA Memory is used for two specific types of functions: System Integration functions such as control and status bits or Large Integrated memory functions for handling data, such as FIFOs etc. The new XC4000E with fast Dual-Port RAM efficiently implements both these types of RAM applications. Altera's Flex 10K series with their limited number of Large, Slow and Inflexible RAM block, fails to provide high performance memory functions.

System Integration Functions

Frequently FPGA designs require a multiple, small, fast and flexible memories for system configuration, control and status functions. These memories are usually distributed throughout the design. The XC4000E family fast Select-RAM memory at 4 ns, is ideal for such applications. As in

the XC4000 family, the XC4000E CLBs can be used as memory instead of logic "on demand". These memories can then be linked together for various data width or depth sizes.

Altera's large 2K bit memory blocks are wasteful because all of the memory within a block, is seldom utilized. Also, for most designs all of the blocks can not be utilized, wasting valuable silicon. And they are slow due to their large size; Altera datasheet says 20 ns. The table below compares the XC4000E memory implementation with the Altera Flex 10K for system Integration functions.

For example, when implementing a standard PCI 64 X 8 FIFO the XC4000E allows designers to instantiate multiple FIFOs with no wastage (see [Figure 1](#) and [Table 1](#)).

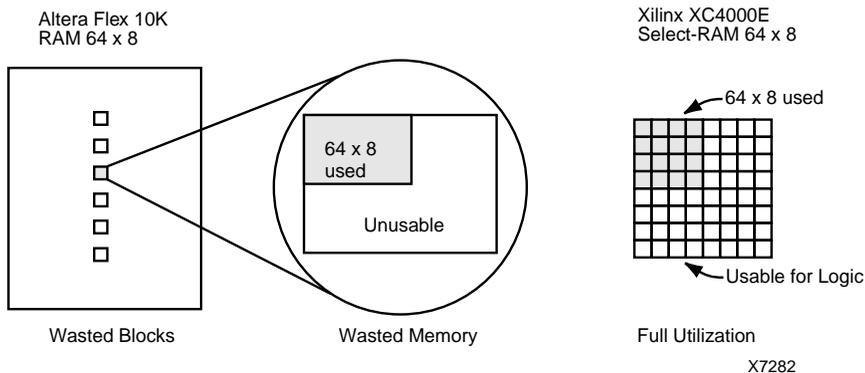


Figure 1: 64 x 8 FIFO Memory Utilization Comparison

Table 1: Memory Function Summary

Feature	Xilinx 4000E	Altera 10K	Design Impact of 10K
Dual-Port RAM	Dedicated	Emulated	- Half the Speed - Half the Memory
Performance for FIFO etc.	FAST(5-15 ns)	SLOW (20-40 ns)	- Limited to Slow Applications

Large Integrated Memory Functions

FPGA designs frequently implement large FIFOs/RAM Buffers especially in Datacomm and DSP intensive areas. Most FIFO/RAM Buffer functions require Dual Port RAMs along with fast speed. The Xilinx XC4000E Select-RAM now offers Dual-Port RAMs with independent access from both sides.

The Altera Flex 10K requires emulating dual-port RAM which cuts down the available memory size and speed in half! This makes a 20ns memory operate on certain key timings at a slow 40ns speed, eliminating a number of fast speed applications (see Table 1). The limited interconnect

capability of Flex devices complicates this (see Application Brief XBRF 003) further slowing down the effective performance. Once again XC4000E with dual port RAM offers fast performance to address leading edge designs.

Finally Altera claims that the large memory blocks can be used for logic functions. At 20 ns speeds the RAM blocks implement slower logic than PALs used to do five years ago. t_{PD} from input to output using Altera 10K for simple Address Decodes will take over 30 ns. That is four times longer than what a 386 microprocessor required five years ago!

Table 2: Select-RAM Feature Summary

Feature	Xilinx 4000E	Altera 10K	Design Impact of 10K
Flexibility	High	Low Large & Inflexible	Inflexible For Configuring Different Sizes Wasteful For Most Applications
Logic/Memory Trade-off	Logic or Memory On-Demand!	No Choice!	Unused blocks wasted
Performance	FAST (4-10 ns)	SLOW (20 ns)	Limited to Slow Applications!



Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
U.S.A.
Tel: 1 (800) 255-7778
or 1 (408) 559-7778
Fax: 1 (800) 559-7114
Net: hotline@xilinx.com
Web: http://www.xilinx.com

North America

Irvine, California
(714) 727-0780

Englewood, Colorado
(303)220-7541

Sunnyvale, California
(408) 245-9850

Schaumburg, Illinois
(847) 605-1972

Nashua, New Hampshire
(603) 891-1098

Raleigh, North Carolina
(919) 846-3922

West Chester, Pennsylvania
(610) 430-3300

Dallas, Texas
(972) 960-1043

Europe

Xilinx Sarl
Jouy en Josas, France
Tel: 011-(33) 1-34-63-01-01
Net: frhelp@xilinx.com

Xilinx GmbH
Aschheim, Germany
Tel: (49) 89-991-5490
Net: dlhelp@xilinx.com

Xilinx, Ltd.
Byfleet, United Kingdom
Tel: (44) 1-932-349401
Net: ukhelp@xilinx.com

Japan

Xilinx, K.K.
Tokyo, Japan
Tel: (03) 3297-9191

Asia Pacific

Xilinx Asia Pacific
Hong Kong
Tel: (852) 2424-5200
Net: hongkong@xilinx.com

© 1996 Xilinx, Inc. All rights reserved. The Xilinx name and the Xilinx logo are registered trademarks, all XC-designated products are trademarks, and the Programmable Logic Company is a service mark of Xilinx, Inc. All other trademarks and registered trademarks are the property of their respective owners.

Xilinx, Inc. does not assume any liability arising out of the application or use of any product described herein; nor does it convey any license under its patent, copyright or maskwork rights or any rights of others. Xilinx, Inc. reserves the right to make changes, at any time, in order to improve reliability, function or design and to supply the best product possible. Xilinx, Inc. cannot assume responsibility for the use of any circuitry described other than circuitry entirely embodied in its products. Products are manufactured under one or more of the following U.S. Patents: (4,847,612; 5,012,135; 4,967,107; 5,023,606; 4,940,909; 5,028,821; 4,870,302; 4,706,216; 4,758,985; 4,642,487; 4,695,740; 4,713,557; 4,750,155; 4,821,233; 4,746,822; 4,820,937; 4,783,607; 4,855,669; 5,047,710; 5,068,603; 4,855,619; 4,835,418; and 4,902,910. Xilinx, Inc. cannot assume responsibility for any circuits shown nor represent that they are free from patent infringement or of any other third party right. Xilinx, Inc. assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made.