

# New HDLC and ADPCM Cores

## A strategic partnership with ISS produces advanced communications products.

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To help our customers reduce design cycles and get products to market quickly, Xilinx and ISS (Integrated Silicon Systems, Ltd.) have entered into a strategic development and OEM agreement to provide versions of ISS multimedia and communications cores optimized for Xilinx FPGAs. The IP cores will be available for purchase from Xilinx as LogiCORE products, downloadable from the Xilinx IP Center, and optimized for Xilinx architectures and design tools. The cores in this program include Single-channel HDLC, 32-channel HDLC, and 32-channel ADPCM, and are available now.

### A Strategic Alliance

The deliverables of this agreement are optimized and supported cores from ISS's

extensive IP portfolio for the latest Xilinx devices including Virtex, Virtex-E, and Spartan-II FPGAs, as well as future FPGA families. Xilinx will deliver these LogiCORE products using the Xilinx



CORE Generator tool to smoothly integrate the cores into the Xilinx design flow.

“This agreement broadens our long-term and successful relationship with Xilinx,” said James G. Doherty, CEO of ISS. “The strength of the Xilinx Virtex architecture coupled with their commitment to partner-

ships provides a perfect environment to expand the usage of ISS cores in wireless and wired communications, and digital video and imaging applications. With this agreement, Xilinx can now fully utilize our expertise in multimedia communications to provide the highest-performance, off-the-shelf design solutions available in the market.”

“ISS has achieved industry-wide recognition for solving the needs of the communications and multimedia user community,” said Mark Aldering, senior director for the IP Solutions Division at Xilinx. “By partnering with ISS, Xilinx is able to address the demand for a one-stop source of high-quality, cost-effective, optimized FPGA cores. This agreement expands the successful long-term relationship between ISS and Xilinx, which started with membership in the Xilinx

AllianceCORE third party IP development program and the co-development partnership for Reed-Solomon Forward Error Correction cores. The agreement reinforces the Xilinx commitment to providing leading-edge IP for multi-million gate FPGA designs.”

### The New Cores

The first three cores to result from the Xilinx-ISS agreement are focused on accelerating the design cycle of high-density FPGAs in communications applications.

**“THE STRENGTH OF THE XILINX VIRTEX ARCHITECTURE, COUPLED WITH THEIR COMMITMENT TO PARTNERSHIPS, PROVIDES A PERFECT ENVIRONMENT TO EXPAND THE USAGE OF ISS CORES IN WIRELESS AND WIRED COMMUNICATIONS, AND DIGITAL VIDEO AND IMAGING APPLICATIONS.”**

The HDLC (High-level Data Link Control) protocol controller cores and the ADPCM (Adaptive Differential Pulse Code Modulation) codec core are used in a number of telecom applications ranging from internet routers and switches to VoIP (Voice over Internet Protocol) gateways.

“The Xilinx HDLC and ADPCM LogiCORE products address the exploding demand from telecom and network developers for complex Virtex-based IP for data and voice processing,” said Babak Hedayati, Director of Marketing and Business Development at Xilinx IP Solutions Division. “The HDLC protocol is proven as one of the most popular methods of transmitting data over WAN systems. The availability of these cores on the Xilinx IP Center provides a one stop source to integrate telecom IP solutions into Xilinx FPGAs.”

### HDLC Cores

The HDLC cores conform to the ITU Q.921 and X.25 recommendations for full duplex, point-to-point and multi-point operation. The cores function at data rates over 40 Mbps and include a direct connection to pulse code modulation (PCM) networks. The HDLC cores are ideal for public and private packet switched data networks such as Frame Relay switches, cable modems, Broadband ISDN, T1/E1, T3/E3, Packet-based DSL Access Multiplexers (DSLAMs), Remote/multi-service access concentrators, and Sonet networks.

### ADPCM Cores

The 32 Channel ADPCM speech codec performs the ITU G.726 conversion of 64 kbit/s A-law or  $\mu$ -law PCM channels to and from 40-, 32-, 24- or 16-Kbit channels using the Adaptive Differential Pulse Code Modulation transcoding technique. The core supports up to 32 duplex encoding/decoding channels or up to 64 encoding and/or decoding channels, and can operate in burst or continuous modes. It is on-line configurable for A-law or  $\mu$ -law PCM encoding as well as various ADPCM compression rates including G.721 or G.723 mode operation. The ADPCM codec will be used in applications such as CO DSLAMs, satellite communications, digital audio storage, H.323 VoIP gateways, access servers, and computer telephony and cellular networks where high quality voice compression is important.

### Availability

The HDLC and ADPCM cores are available now. Suggested resale pricing is \$7,200 for the 32 Channel HDLC controller core, \$3,900 for the Single Channel HDLC controller core, and \$14,400 for the 32 Channel ADPCM codec core. Licensing information and instructions for downloading the cores, and information on all Xilinx LogiCORE products can be found at the Xilinx IP Center at: [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter). Information on other Xilinx LogiCORE and third-party AllianceCORE products is also available from the IP Center.

### Conclusion

The strategic partnership between Xilinx and ISS is already producing optimized cores for the communications market, and many more are on the way. Xilinx continues to provide the most advanced FPGA and IP technologies to help you create the next generation of high performance equipment and get your products to market as soon as possible.

## About ISS

Integrated Silicon Systems Ltd. (ISS) is the leading supplier of application-specific virtual components (ASVCs) for multimedia and communications FPGA, ASIC, and System-on-a-Chip (SoC) integrated circuits. ISS delivers video/image compression, audio compression, and channel coding solutions for consumer and communications applications. Using proprietary techniques for direct-mapped implementations of digital signal processing functions and algorithms in hardware, ISS delivers solutions that realize 10X to 1000X improvements in performance compared to conventional implementations using software-programmable DSP microprocessors. ISS is a privately held company with European headquarters in Belfast, Northern Ireland, UK and worldwide sales and marketing operations in San Jose, California. More information about ISS and its products may be obtained at <http://www.iss-dsp.com>