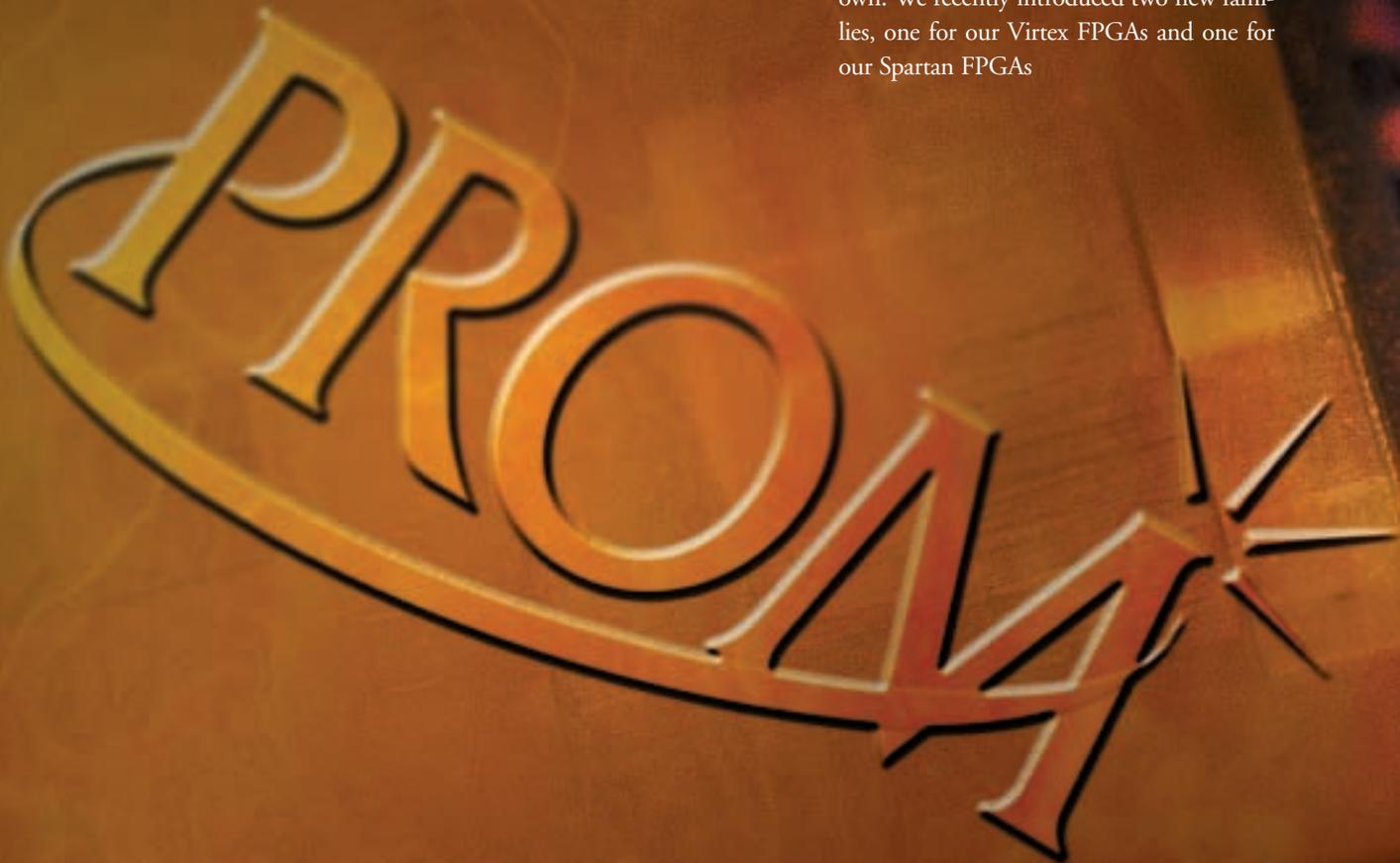


# New High-Density Virtex PROMs and Cost-Effective Spartan-II PROMs

Xilinx announces the addition of the XC17V00 and XC17S00A families to its existing line of one-time programmable (OTP) PROMs.

by Theresa Vu  
Product Marketing Engineer, Xilinx Inc.  
theresa.vu@xilinx.com

All Xilinx PROM families are designed specifically for use with Xilinx FPGAs, therefore we offer a complete, pre-engineered, drop-in configuration solution that works perfectly the first time; and you are spared the time-consuming task of designing your own. We recently introduced two new families, one for our Virtex FPGAs and one for our Spartan FPGAs



### Virtex Configuration PROMs



Our low-cost XC17V00 PROMs support Virtex and Virtex-E FPGAs, up to 3.2 million system gates, and are offered in 1-Mb to 16-Mb densities. The available packages are shown in Table 1.

The 16-Mb 17V16 PROM, a four-fold increase in maximum bit density, extends the Xilinx leadership in configuration memories and provides a one-chip configuration solution for our entire line of Virtex FPGAs.

#### Key Features

The XC17V00 serial/parallel PROM family is based on our proven, OTP architecture that provides a stable, low-cost, highly-reliable one-chip configuration solution with the following features:

- 1-Mb to 16-Mb densities.
- Simple, fast, serial FPGA interface that requires only one user I/O pin.
- Parallel configuration up to 264 Mbps (17V16 and 17V08 only).
- Available in SOIC, VOIC, VQFP, and PLCC packages.
- Low-power CMOS floating gate process.
- Programming support by leading programmer manufacturers.
- Cascadable for storing longer or multiple bitstreams.

Device	Density	8-pin VOIC	20-pin SOIC	20-pin PLCC	44-pin PLCC	44-pin VQFP
XC17V01	1.6Mb	✓	✓	✓		
XC17V02	2Mb			✓	✓	✓
XC17V04	4Mb			✓	✓	✓
XC17V08	8Mb				✓	✓
XC17V16	16Mb				✓	✓

Table 1 - Virtex PROM packages

XCV300E	▼▼▼▼▼▼▼▼
XCV400E	▼▼▼▼▼▼▼
XCV405E	▼▼▼▼▼▼
XCV600E	▼▼▼▼▼
XCV812E	▼▼▼
XCV1000E	▼▼▼
XCV1600E	▼▼▼
XCV2000E	▼▼
XCV2600E	▼▼
XCV3200E	▼▼

Table 2 - Number of Virtex-E FPGAs configurable by one 16Mb PROM

FPGA	PROM Solution	8-pin PDIP	8-pin VOIC	20-pin SOIC	44-pin VQFP
XC2S15	XC17S15A	✓	✓	✓	
XC2S30	XC17S30A	✓	✓	✓	
XC2S50	XC17S50A	✓	✓	✓	
XC2S100	XC17S100A	✓	✓	✓	
XC2S150	XC17S150A	✓	✓	✓	
XC2S200	XC17S200A	✓	✓		✓

Table 3 - Spartan-II PROM packages and device compatibility

### The Most Cost-effective Solution

The new XC17V00 family also offers significant savings in board space, design time, and cost. Using one 17V16 to configure the new 3.2 million system-gate Virtex XCV3200E FPGA requires less than one fourth the board space of any previous Xilinx configuration PROM solution. To get the equivalent functionality from our nearest competitor would require 14 chips and more than 2x the board space, as illustrated in Figure 1.

Xilinx process expertise has also allowed us to use smaller packages, further reducing the need for board space.

### Configuration of Multiple FPGAs

The XC17V16 can also be used to configure multiple, daisy-chained FPGAs. This allows you to store configuration data for up to eight FPGAs in a single PROM, as illustrated in Table 2.

### Spartan-II Configuration PROMs



Our XC17S00A PROM Family provides a high-performance, low-cost configuration solution, optimized

for use with Spartan-II FPGAs. This family offers a dedicated PROM for each gate density in the Spartan-II family for ease-of-selection and guaranteed compatibility, as shown in Table 3. This family also offers extended availability of the smallest package offered by Xilinx, the 8-pin VOIC.

#### Key Features

- Simple, fast, serial Spartan FPGA interface that requires only one user I/O pin.
- Available in DIP, VOIC, SOIC, and VQFP packages.
- Advanced, low-cost CMOS process.
- Programming support by leading programmer manufacturers.

#### Conclusion

With the new XC17V00 and XC17S00A PROMs, there is no easier, faster, or less expensive way to configure Xilinx FPGAs. For more information see: [www.xilinx.com](http://www.xilinx.com).

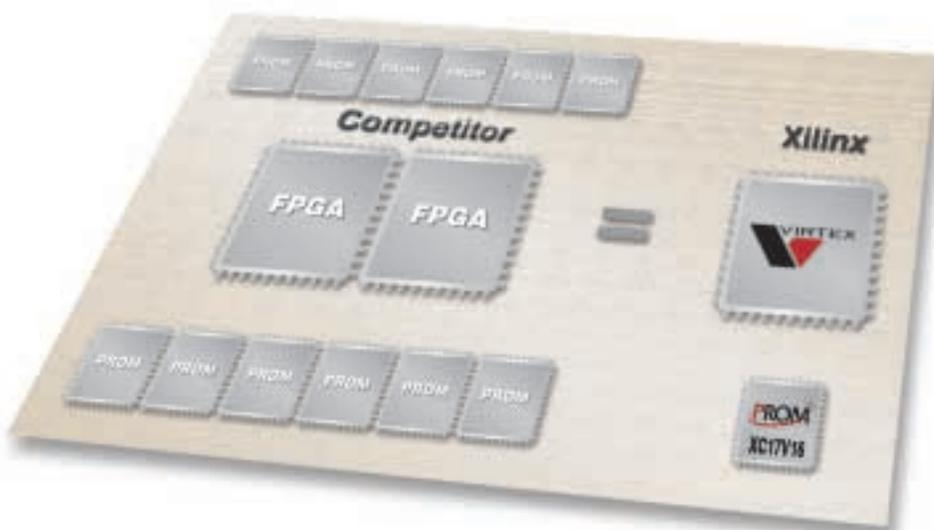


Figure 1 - The Xilinx solution beats the competition