Dual-Port Block Memory for Virtex and Virtex-II V3.0

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Features

- Fully synchronous drop-in modules for the Virtex™ and Virtex™-II families; uses Virtex or Virtex-II block memory for performance and efficiency.
- Supports all three Virtex-II write mode options: read after write, read before write, and no read on write (available only for Virtex-II implementation).
- Supports data widths from 1 to 256 bits.
- Supports memory depths from 2 to 256K words for Virtex and from 2 to 1M words for Virtex-II.
- Supports ROM functions, enabling simultaneous read operations from the same location.
- Supports RAM functions, enabling simultaneous write operations to separate locations and simultaneous read operations from the same location.
- The ports are completely independent of each other.
- Supports asymmetric A and B port configurations.
- Available in the XIlinx CORE Generator™ System V3.1i.

Functional Description

The Dual-Port Block Memory module for Virtex is composed of single or multiple Virtex 4Kb blocks called SelectRAM+™. The Dual-Port Block Memory module for Virtex-II, on the other hand, is composed of single or multiple Virtex-II 18Kb blocks (SelectRAM-II™) enabling deeper and/or wider memory implementations. Both the SelectRAM+ and SelectRAM-II memories are True Dual-Port™ RAM, offering fast, discrete, and large blocks of memory in the Virtex device family.

A memory module has two independent ports that enable shared access to a single memory space and which are generated based on user-defined width and depth. Both ports are functionally identical, with each port providing read and write access to the memory. Simultaneous reads

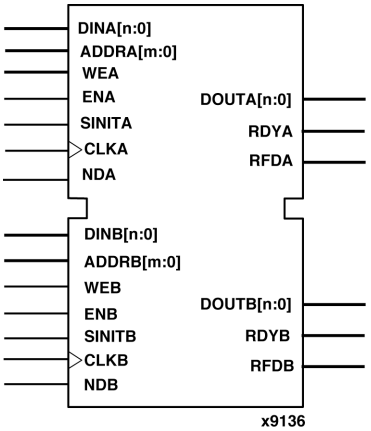

Figure 1: Core Schematic Symbol

from the same memory location may occur, but all other simultaneously reading-from and writing-to the same memory location will result in correct data being written into the memory, but invalid data being read.

The memory's Port A and Port B are configured to support user-defined data input and address widths. When both ports are disabled (ENA and ENB inactive) the memory contents and output ports remain unaltered. When either port is enabled (ENA or ENB asserted) all memory operations occur on the rising edge of the clock input.

During a write operation (WEA or WEB asserted), the data presented at the port's data input is stored in memory at the location selected by the port's address input. During this operation, the data output port behaves differently for the Virtex and Virtex-II architectures.

The data output port of the Virtex-II implementation is dependent on a chosen "write mode" option. Three "write mode" options are supported by the Virtex-II architecture. Each of these options determines the behavior of the corresponding data output port when a write operation occurs.

The Virtex implementation, on the other hand, supports a single "write mode" option: Read-After-Write. This "write mode" causes the current data in the addressed memory location to be transferred to the data output port when a write operation occurs.

During a read operation, the memory contents at the location selected by the address will appear at the module's output. When Synchronous Initialization (SINITA or SINITB) is active, the module's registered outputs are syn-

chronously reset to zero for Virtex and to a user-defined value for Virtex-II. The synchronous Initialization command has no effect on the contents of the memory, and write operations may still take place. For additional information on the Virtex and Virtex-II BlockRAM, refer to the respective *Virtex* or *Virtex-II Handbook,* available at http://www.xilinx.com/products/virtex/v2handbook.htm.

Pinout

Port names for the core module are shown in Figure 1 and defined in Table 1. The inclusion of some ports on the module is optional; exclusion of these ports will alter the function of the module. The optional ports are marked in Table 1 and described in more detail below.

Clock Enable - CLK[AIB]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the rising edge of their corresponding CLK pin. The data bus has a clock-to-out time referenced to the CLK pin. If a falling edge operation is required, the user should invert the clock signal attached to the core's clock ports.

Enable - EN[AIB]

The enable pin affects the read, write, and SINIT functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory locations.

Write Enable - WE[AIB]

Activating the write enable pin allows the port to write to the memory locations. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (write first, read first, no change). When inactive, a read operation occurs, and the contents of the memory locations referenced by the address bus reflect on the DOUT bus, regardless of the write mode selected.

Synchronous Initialization - SINIT[AIB]

The SINIT pin forces the data output ports to a SINIT value. For the Virtex implementation, the SINIT value is zero, and for the Virtex-II implementation the SINIT value is user-defined. The data output ports are each synchronously asserted to their respective SINIT value. This operation does not affect memory locations and does not disturb write operations on the other port. If the core is configured with an enable pin, the SINIT function is active only when the enable port is active.

Address Bus - ADDR[AIB]<m:0>

The address bus selects the memory location that will be accessed during a read or write operation.

Table 1: Core Signal Pinout

SIgnal	Direction	Description
DIN[A|B]<n:0> (Optional)	Input	**Data Input**: data to be written into memory via Port [A|B].
ADDR[A|B]<m:0>	Input	**Address**: the memory location to which data will be written or read via Port [A|B].
WE[A|B] (Optional)	Input	**Write Enable**: control signal used to allow transfer of input data into memory via Port [A|B] (Active High).
EN[A|B] (Optional)	Input	**Enable**: control signal used to enable memory accesses via read and write operations from Port [A|B] (Active High).
SINIT[A|B] (Optional)	Input	**Synchronous Initialization**: control signal used to force the module's outputs to a predefined state (Active High).
CLK[A|B]	Input	**Clock**: clock input, all memory access is synchronous with the clock input.
ND[A|B] (Optional)	Input	**New Data Port A**: indicates that there is a new and valid address on Port ADDR[A|B] (Active High).
DOUT[A|B]<n:0> (Optional)	Output	**Data Output**: synchronous output of memory.
RFD[A|B] (Optional)	Output	**Ready for Data**: indicates that the memory is ready to accept new data (Active High).
RDY[A|B] (Optional)	Output	**Ready**: indicates valid data on port DOUT [A|B] (Active High).

Data-In Bus - DIN[AIB]<n:0>

The DIN buses provide the new data value to be written into the memory. Data input and output signals are always busses; that is, in a 1-bit width configuration, the data input signal is DIN[0] and the data output signal is DOUT[0].

Data-Out Bus - DOUT[AIB]<n:0>

The DOUT buses reflect the contents of memory locations referenced by the address bus during a read operation.

During a write operation of a Virtex memory (read first configuration), the DOUT buses reflect the stored value before the write.

During a write operation of a Virtex-II memory (write first or read first configuration), the DOUT buses reflect either the

DIN buses or the stored value before write. During a write operation of a Virtex-II memory in no change mode, DOUT buses are not affected.

New Data - ND[AIB]

ND indicates that there is a new and valid address on ADDR[A|B] port. It affects only the RDY port.

Ready for Data - RFD[AIB]

RFD indicates that the memory is ready to accept new data. RFD[A|B] is always true, except when EN[A|B] is inactive.

Output Ready (valid) - RDY[AIB]

Indicates valid output on port DOUT[A|B] relative to when ND is asserted. RDY[A|B] will lag ND[A|B] by the latency of the block memory.

CORE Generator Parameters

The CORE Generator parameterization windows for this module are shown in Figure 2 and Figure 3. These windows are interactive to allow user-defined customization of the Block Memory. In Figure 2, the configuration for Port A and Port B can be customized. An information window, shown at the bottom, verifies that the total number of blocks required does not exceed those available on the targeted device. In Figure 3, several other design options are available, including optional pins and pipelining.

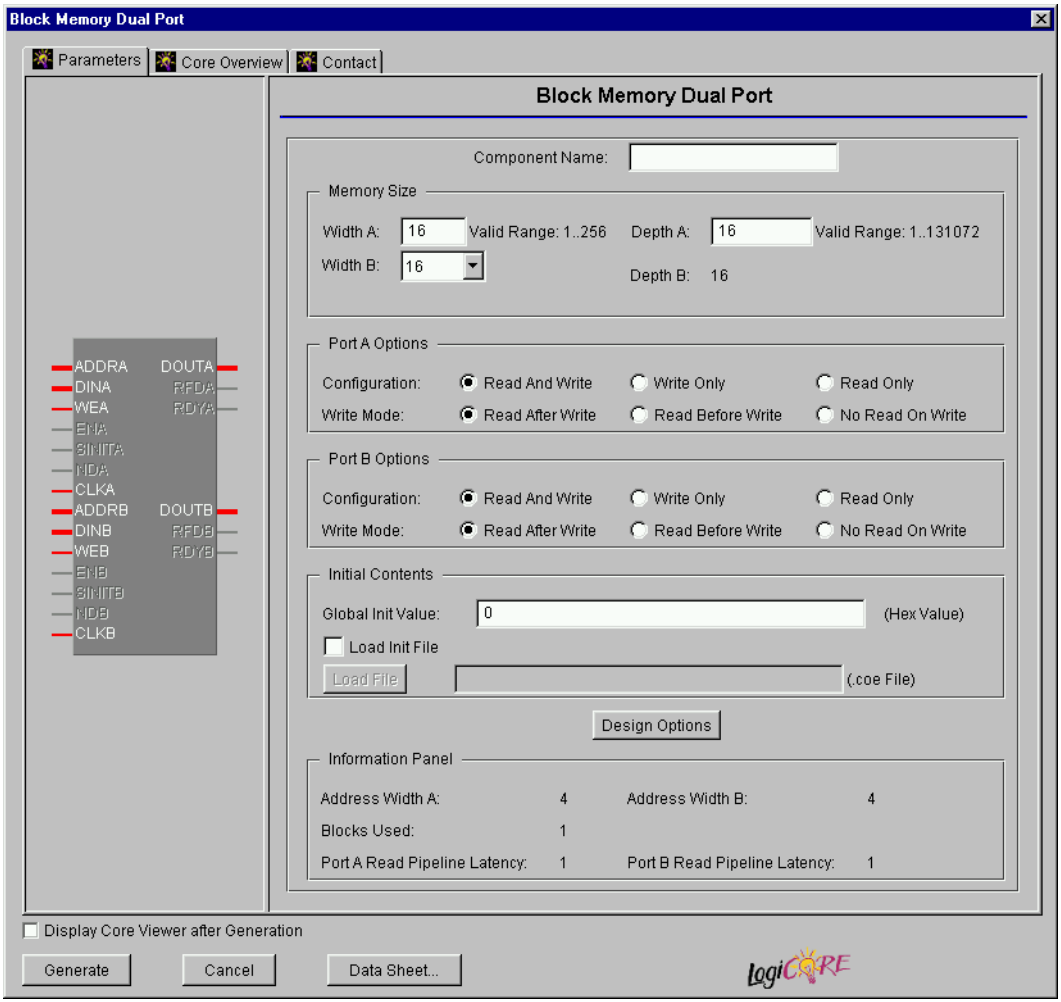

Figure 2: Dual-Port Block Memory Main Parameterization Window

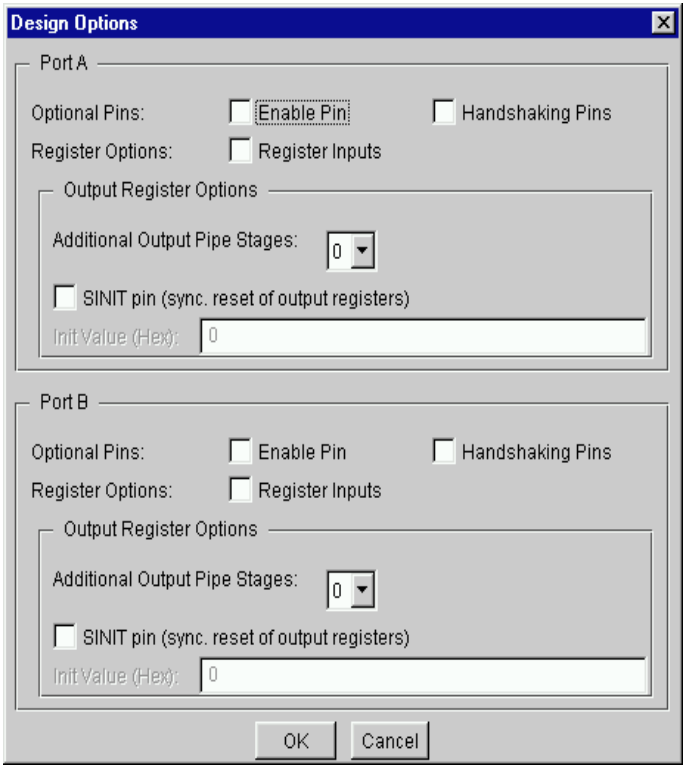

Figure 3: Dual-Port Block Memory Design Options Window

Definition of GUI Interface Fields

- **Component Name**: Enter a name for the output files generated for this module (up to 256 characters).
- **Memory Size - Port A**:
  - **Width A**: Select the data bit width. The width can be between 1 and 256.
  - **Depth A**: Select the number of words in memory. The value range is 2 to 262,144 (256K) for Virtex and 2 to 1,048,576 (1M) for Virtex-II. Available depths will vary depending on the width entered for Port A; the absolute maximum number of words is 256K for the Virtex architecture and 1M for the Virtex-II architecture. Be aware that cores should not exceed the number of Block RAM primitives in the targeted device.
- **Memory Size - Port B**:
  - **Width B**: Select the data bit width. Available widths will vary depending on the width entered for port A. For the Virtex architecture, the available widths could be 1, 2, 4, 8 and 16 times larger than the width entered for port A. The available widths for the Virtex-II architecture could be 1,2,3,8,16 and 32 times larger than the width entered for port B.
  - **Depth B**: Reports the depth of Port B. This value is calculated such that Port A and Port B have the same memory size.
- **Port A Options**:
  - **Configuration**:
    - **Read and Write**: Configures Port A to have DINA and DOUTA ports allowing read and write access to the memory.
    - **Write Only**: Configures Port A to have a DINA port enabling this port to be used only for write access. Note that only one port can be configured to be Write Only.
    - **Read Only:** Configures Port A to have a DOUTA port enabling this port to be used for read only access. Note that only one port can be configured to be Read Only.
  - **Write Mode**: Select one for Virtex-II architecture. The default is Read-After-Write. The Virtex architecture supports only Read-After-Write.
    - **Read after Write**:
    - (1) No Inputs or Outputs Registered: The input data is transferred onto the DOUTA port on the rising clock edge immediately following the assertion of the WEA input.

- (2) With Inputs Registered Only: The input data is transferred onto the DOUTA port on the second rising clock edge immediately following the assertion of the WEA input.
- (3) With Outputs Registered: The input data is transferred onto the DOUTA port on the second rising clock edge immediately following the assertion of the WEA input.
- (4)With Inputs and Outputs Registered: The input data is transferred onto the DOUTA port on the third rising clock edge immediately following the assertion of the WEA input.
- **Read before Write**:
- 1) No Inputs or Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the rising clock edge immediately following the assertion of the WEA input.
- (2) With Inputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the second rising clock edge immediately following the assertion of the WEA input.
- (3) With Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the second rising clock edge immediately following the assertion of the WEA input.
- (4)With Inputs and Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the third rising clock edge immediately following the assertion of the WEA input.
- **No Read on Write**:
- A read operation is not performed when WEA is asserted. The DOUTA port will contain the contents of the last read memory location.

- **Port B Options**:
  - **Configuration**:
    - **Read and Write**: Configures Port B to have DINB and DOUTB ports allowing read and write access to the memory.
    - **Write Only**: Configures Port B to have a DINB port enabling this port to be used only for write access. Note that only one port can be configured to be Write Only.
    - **Read Only**: Configures Port B to have a DOUTB port enabling this port to be used only for read access. Note that only one port can be configured to be Read Only.
  - **Write Mode**:Select one for Virtex-II architecture. The default is Read-After-Write. The Virtex architecture supports only Read-After-Write.
    - **Read after Write**:
    - (1) No Inputs or Outputs Registered: The input data is transferred onto the DOUTB port on the rising clock edge immediately following the assertion of the WEB input.
    - (2) With Inputs Registered Only: The input data is transferred onto the DOUTB port on the second rising clock edge immediately following the assertion of the WEB input.
    - (3) With Outputs Registered: The input data is transferred onto the DOUTB port on the second rising clock edge immediately following the assertion of the WEB input.
    - (4)With Inputs and Outputs Registered: The input data is transferred onto the DOUTB port on the third rising clock edge immediately following the assertion of the WEB input.
    - **Read before Write**:
    - 1) No Inputs or Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the rising clock edge immediately following the assertion of the WEB input.
    - (2) With Inputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the second rising clock edge immediately following the assertion of the WEB input.
    - (3) With Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the second rising clock edge immediately following the assertion of the WEB input.
    - (4)With Inputs and Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the third rising clock edge immediately following the assertion of the WEB input.
    - **No Read on Write**:
    - A read operation is not performed when WEB is asserted. The DOUTB port will contain the contents of the last read memory location.
- **Initial Contents**: Enter the parameter fields related to the data stored in the memory directly after device configuration. Note that these initial data must conform to the chosen Port A parameter fields.
  - **Global Init Value**: Enter the value to be stored in any memory location not specified by another means. When no values are entered, this field defaults to 0. Value must be in Hex. This value must be smaller than Port A's largest word.
  - **Load Init File**: Select this if the initial contents of the memory are to be read from a *coe* file.
  - **Load File**: Press this button to activate a browser window that lets the user pick a coefficient or *coe* file that contains the initial contents of the memory. This is an ASCII file with a ".coe" extension. For further information regarding the memory's initial contents, refer to the *Specifying Memory Contents* section.

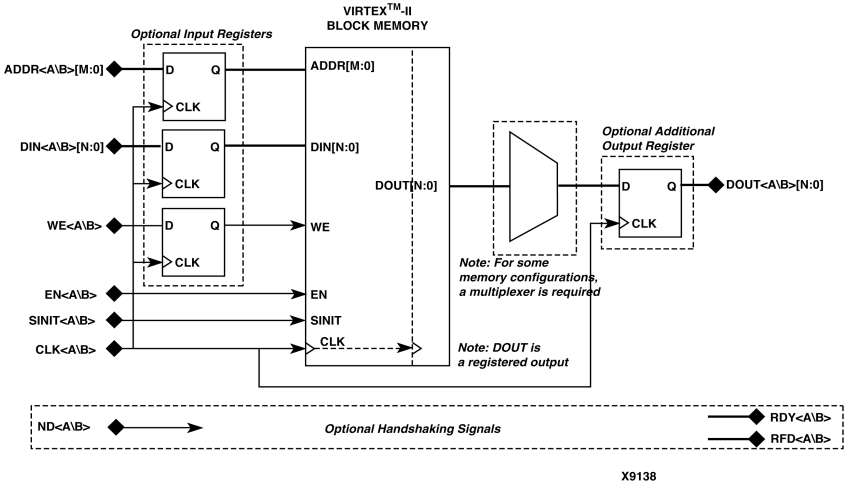

Figure 4: Dual-Port Memory Block Diagram

- **Design Options**: Select to open another window with additional configuration options.
- **Information Panel**: Lists the resulting configuration of the core.
  - **Address Width A**: Displays the number of address bits required for Port A for this configuration.
  - **Address Width B**: Displays the number of address bits required for Port B for this configuration.
  - **Blocks Used**: Displays the number of BlockRAM primitives needed to implement this configuration. It is recommended to verify that the required number of blocks does not exceed those available in the targeted device.
  - **Port A Read Pipeline Latency**: Displays the total latency of Port A from the point when a new address is presented to the memory to when it becomes a valid output. The total latency will be increased by one if the inputs are registered or if an additional output register is added.
  - **Port B Read Pipeline Latency**: Displays the total latency of Port B from the point when a new address is presented to the memory to when it becomes a valid output. The total latency will be increased by one if the inputs are registered or if an additional output register is added.
- **Generate**: Select to generate the block memory module. Make sure that the parameters are correctly selected for the particular application before executing this option.
- **Cancel:** Select to close window and return to the Core Generator.
- **Datasheet:** Select to open a PDF version of this document.

Design Options

Port A or Port B

- **Optional Pins**:
  - **Enable Pin**: Check the box to include the enable EN[A\B] port on the module; uncheck the box to remove it.
  - **Handshaking Pin**: Check the box to include the following ports; uncheck the box to remove them.
    - **ND** [New Data]: Signals a new and valid memory address when active.
    - **RFD** [Ready For Data]: Indicates that the memory can accept new addresses.
    - **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid.
- **Register Options**:
  - **Register Inputs**: Check this box to register ports DIN, ADDR, and WE prior to accessing block memory. See Figure 4.
- **Output Register Options:**
  - **Additional Output Pipe Stages**: Select “1” to enable an additional register on the output of the memory; select “0” to disable an additional register on the output of the memory. See Figure 4.
  - **SINIT Pin**: Check box to add the synchronous port SINIT to the memory.
- **Init Value** (HEX value): For Virtex-II architecture, enter the HEX value that the output port will be set to when the SINIT port is true. For Virtex architecture, the Init Value is fixed to 0.
- **Close**: Select to close window and return to the main parameterization window.

Operating Modes

The Virtex-II block SelectRAM-II can maximize the utilization of the True Dual-Port memory at each clock edge by supporting three different write modes. Each port's write mode is independently configurable. The Read-Before-Write mode offers the flexibility of using the data output bus during a write operation on the same port. Output port behavior is determined by the configuration. This choice increases the effective bandwidth of the Block Memory. Note that the Virtex SelectRAM+ supports only the Read-Before-Write mode.

Read Operations

Read operations are synchronous to the rising edge of the clock. The data in the memory location selected by the address appears on the DOUT port after the rising edge of the clock.

Write Operations

Write operations are synchronous to the rising edge of the clock. The data on the DIN port is written into the memory location selected by the address on the rising edge of the clock when WE is active. The user can configure the memory in one of three ways to determine the behavior of the DOUT port during a write cycle. Each port's write mode is independently configurable. Note that the timing diagram and description of the write modes below assume that the memory has been configured without input registering and additional output registers.

Write First or Read-After-Write Mode

In write first mode, data input is loaded simultaneously with a write operation on the DOUT port. As shown in Figure 5, the data input is stored in memory and mirrored on the output.

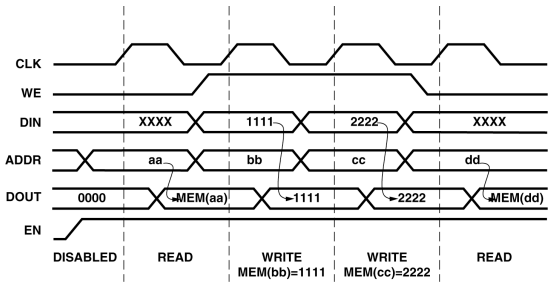

Figure 5: Write First Mode Waveform

Read First or Read-Before-Write Mode

In read first mode, data previously stored at the write address appears on the DOUT port. Data input is stored in memory and the prior contents of that location is driven on the output, during the same clock cycle (shown in Figure 6).

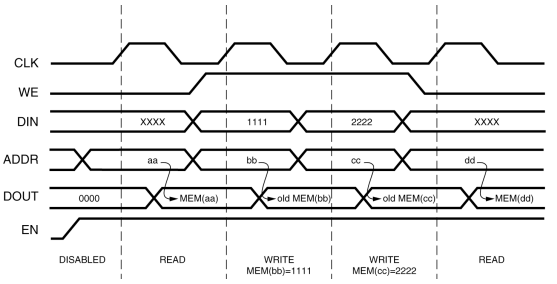

Figure 6: Read First Mode Waveform

No Change or No Read-on-Write Mode

In No Read-on-Write mode, the DOUT port remains unchanged during a write operation. As shown in Figure 7, data output is still the last read data and is unaffected by a write operation on the same port. Mode configuration is static. One of these three modes is set individually for each port by an attribute. The default mode is write first.

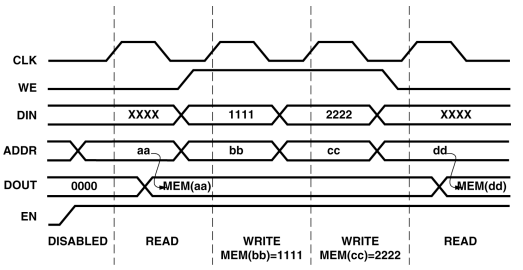

Figure 7: No Read-on-Write Mode Waveform

Conflict Resolution

The Virtex and Virtex-II block memory is True Dual-Port RAM that allows both ports to simultaneously access the same memory location. When one port writes to a given memory location, the other port must not address that memory location (for a write/read) within the clock-to-clock setup window. Note that conflicts do not cause any physical damage to BlockRAM cells. For more information on conflict resolution, refer to the Virtex and Virtex-II Handbook (http://www.xilinx.com/products/virtex/v2handbook.htm).

Specifying Memory Contents

The initial contents of the memory can be assigned by specifying the desired information in a separate text file called a *coe* file. To select and load a *coe* file, press the "Load Init Values..." button on the parameterization window and choose the desired file from the "from" dialog box. An example of a *coe* file for a 3 by 16 RAM is shown in Figure 8.

```
memory_initialization_radix=16;
memory_initialization_vector=123, 456, aaaa;
```

Figure 8: An Example of a COE File for a Virtex-II Single-Port Block RAM

When specifying the initial contents for a memory in a *coe* file, the keywords MEMORY_INITIALIZATION_RADIX and MEMORY_INITIALIZATION_VECTOR can be used. The MEMORY_INITIALIZATION_VECTOR takes the form of a sequence of comma-separated values, one value per memory location, terminated by a semicolon. Any amount of white space, including new lines, can be included in the vector to enhance readability. The format of an individual value in the vector will depend on the MEMORY_INITIALIZATION_RADIX value, which can be 2, 10, or 16 (the default value is 16). The vector must be consistent with the MEMORY_INITIALIZATION_RADIX value and must fall within the range of 0 to 2^{DATA_WIDTH} -1. Values must not be negative.

Core Resource Utilization

The number of Block RAM primitives required is dependent on the values of the data depth and width fields selected in the CORE generator parameterization window, and is at least: (depth x width)/18432 and will exceed this number for many configurations.

For some memory depths, extra logic is required to decode the address and multiplex the outputs from various primitives. Virtex-II CLB slices are used to provide this functionality. The number of slices required depends on the way that the depth is constructed from the primitives, the data width, and the implementation of any decoding or multiplexing.

For more information about the number of block RAMS in each device, please refer to tables 4 through 6.

Table 2: Parameter File Information for Virtex

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width [A|B]	Integer	Ranges from 1 to 256
Depth [A|B]	Integer	Ranges from 2 to 256K
Port Configuration [A|B]	String	Default=read and write Options are: read and write read only write only
Write Modes Port [A|B]	String	Read before Write only
Global Init Value	String	Default=0
Load Init File	Boolean	Default=False False=Use Global Init Value Only True=Use loaded COE file
Coefficient File	String	Default=null
Port [A|B] Enable Pin	Boolean	Default=false
Port [A|B] Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Port [A|B] Register Inputs	Boolean	Default=false
Port [A|B] Additional Output Pipe Stages	Integer	Default=0 0=No additional output registers
Port [A|B] Init Pin	Boolean	Default=false
Port [A|B] Init Value	Integer (Hex)	0 only

Table 3: Parameter File Information for Virtex-II.

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width [A|B]	Integer	Ranges from 1 to 256
Depth [A|B]	Integer	Ranges from 2 to 1Meg
Port Configuration [A|B]	String	Default=read and write Options are: read and write read only write only
Write Modes Port [A|B]	String	Default=Read after Write Options are: Read after Write Read before Write No Read on Write
Global Init Value	String	Default=0
Load Init File	Boolean	Default=False False=Use Global Init Value Only True=Use loaded COE file
Coefficient File	String	Default=null
Port [A|B] Enable Pin	Boolean	Default=false
Port [A|B] Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Port [A|B] Register Inputs	Boolean	Default=false
Port [A|B] Additional Output Pipe Stages	Integer	Default=0 0=No additional output registers
Port [A|B] Init Pin	Boolean	Default=false
Port [A|B] Init Value	Integer (Hex)	0 only

Table 4: Virtex Device Block RAM Counts

Devices	# Blocks	Total Block (bits)
xcv50	8	32,768
xcv100	10	40,910
xcv150	12	49,152
xcv200	14	57,344
xcv300	16	65,536
xcv400	20	81,920
xcv600	24	98,304
xcv800	28	114,688
xcv1000	32	131,072

Table 5: Virtex-E Device Block RAM Counts

Devices	# Blocks	Total Block (bits)
xcv50E	16	65,536
xcv100E	20	81,920
xcv200E	28	114,688
xcv300R	32	131,072
xcv400E	40	163,840
xcv600E	72	294,912
xcv1000E	96	393,216
xcv1600E	144	589,824
xcv2000E	160	655,360
xcv2600E	184	753,664
xcv3200E	208	851,968
xcv405E	140	573,440
xcv812E	280	1,146,880

Table 6: Virtex-II Device Block RAM Counts

Devices	# Blocks	Total Block (Kb)
xc2v250	24	432
xc2v500	32	576
xc2v1000	40	720
xc2v1500	48	864
xc2v2000	56	1,008
xc2v3000	96	1,728
xc2v4000	120	2,160
xc2v6000	144	2,592
xc2v8000	168	3,026
xc2v10000	192	3,456

Ordering Information

This core can be downloaded free of charge from the Xilinx IP Center (http://www.xilinx.com/ipcenter) for use with the Xilinx CORE Generator System V3.1i and later. The CORE Generator System tool is bundled with all Xilinx Alliance and Foundation Series Software packages.

To order online, visit the Xilinx Silicon Expresso Cafe at http://toolbox.xilinx.com/cgi-bin/xilinx.storefront/241669816/catalog/1006. Xilinx software can also be ordered through your local Xilinx sales office. Information on the sales office nearest you is available at http://www.xilinx.com/company/sales.htm.