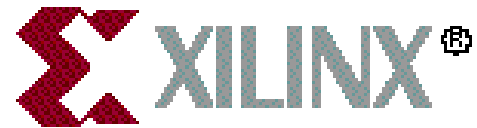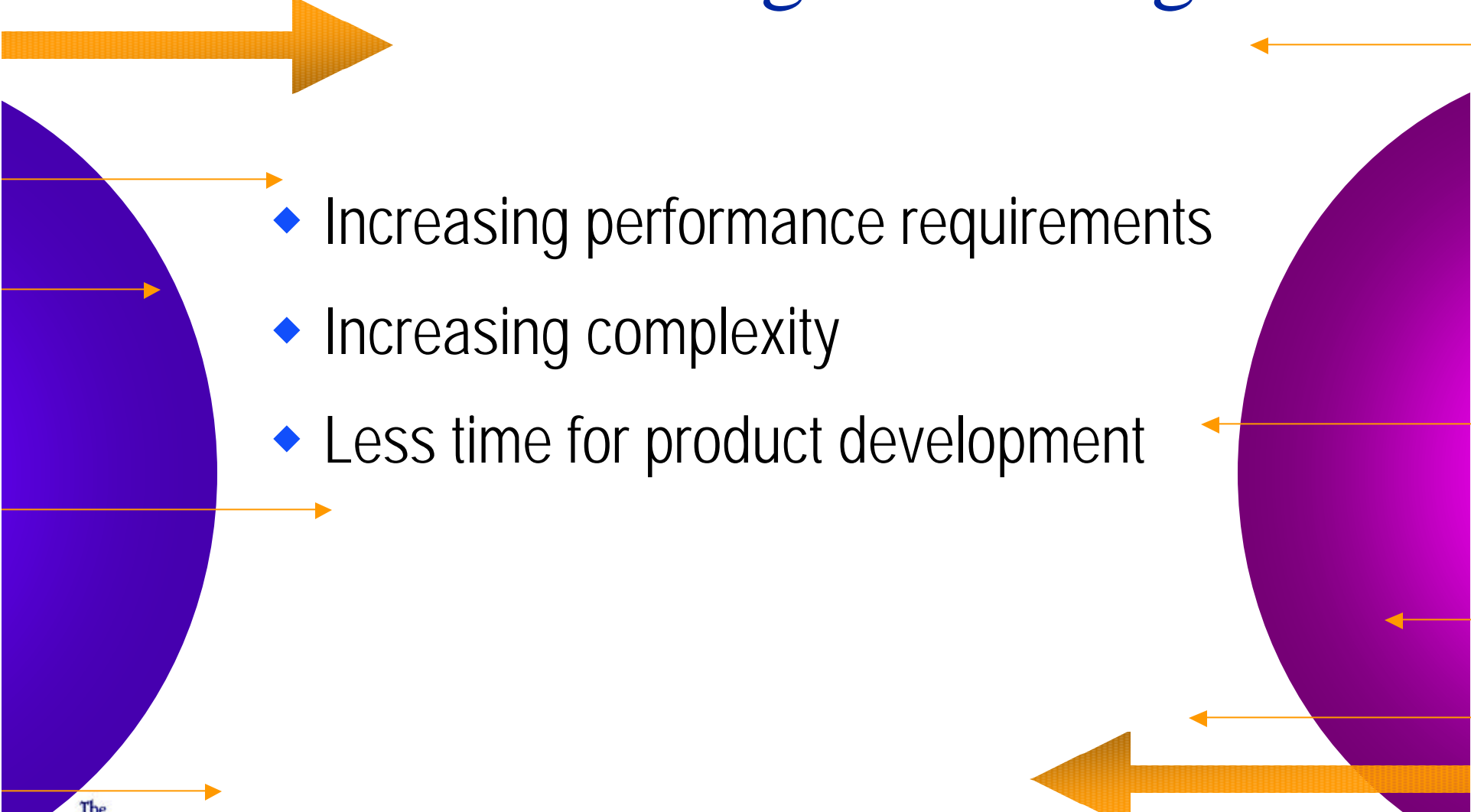# The MathWorks and Xilinx Strategic Alliance

Alliance to Lead the Trend of FPGA-based DSP

- ◆ **Mission**
  - — Enable designers to develop high-performance DSP systems with Xilinx FPGAs using system design and verification tools from The MathWorks, Inc.

- ◆ **Exclusive Strategic Alliance**

- ◆ **First product demonstrated at DSP World**

The DSP Design Challenge

- ◆ Increasing performance requirements

- ◆ Increasing complexity

- ◆ Less time for product development

The MATH WORKS Inc.

XILINX®

The Traditional DSP Alternatives

From the world of
DSP Processors

\+ Quick turnaround

\+ Reconfigurable

\- Relatively low performance

\- Requires additional components

From the world of
ASICs

\+ High-performance

\+ One-chip solutions

\- Long turnaround

\- Cannot be changed

\- Expensive NRE

Xilinx FPGAs Combine the Best of Two Worlds

Xilinx FPGAs

+ Quick turnaround

+ Reconfigurable

+ High-performance

+ One-chip solutions

The MATH WORKS Inc.

XILINX ®

Typical FPGA-based DThe
DSP Design Flow
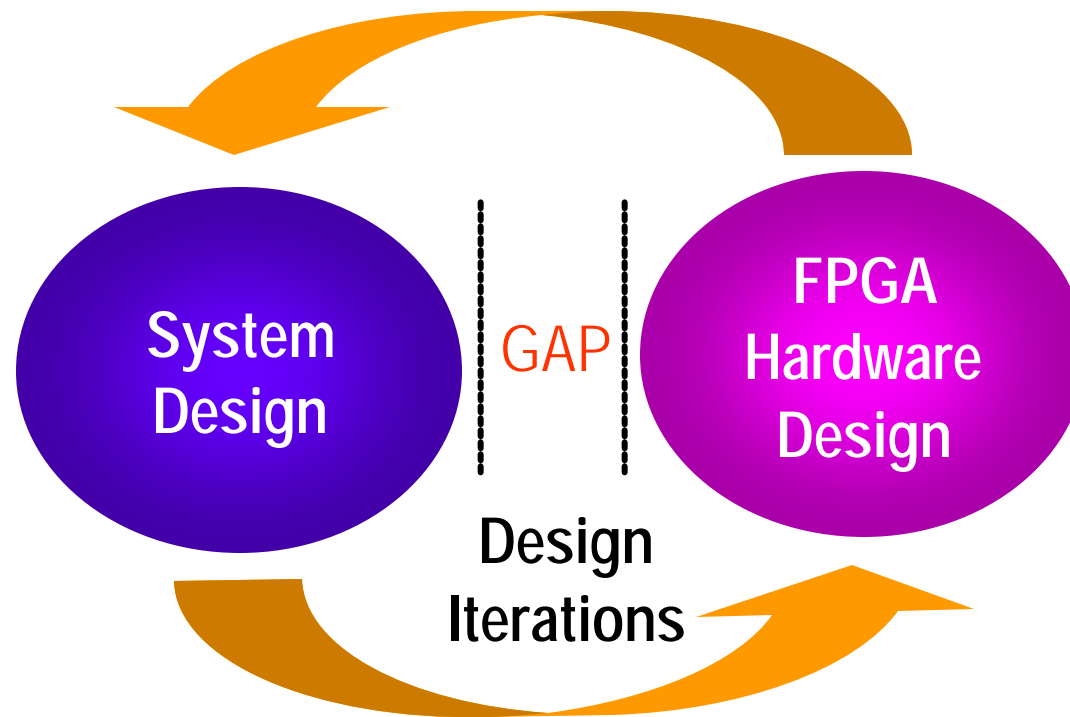
Numerous design iterations to trade-off hardware usage and performance

Typical Design Cycle

Traditional design methodology

System Design → Design Iterations → HW Design

Development Time

Cores Shorten the Design Cycle

Traditional design methodology

System Design → Design Iterations → HW Design

Using cores

System Design → Design Iterations →
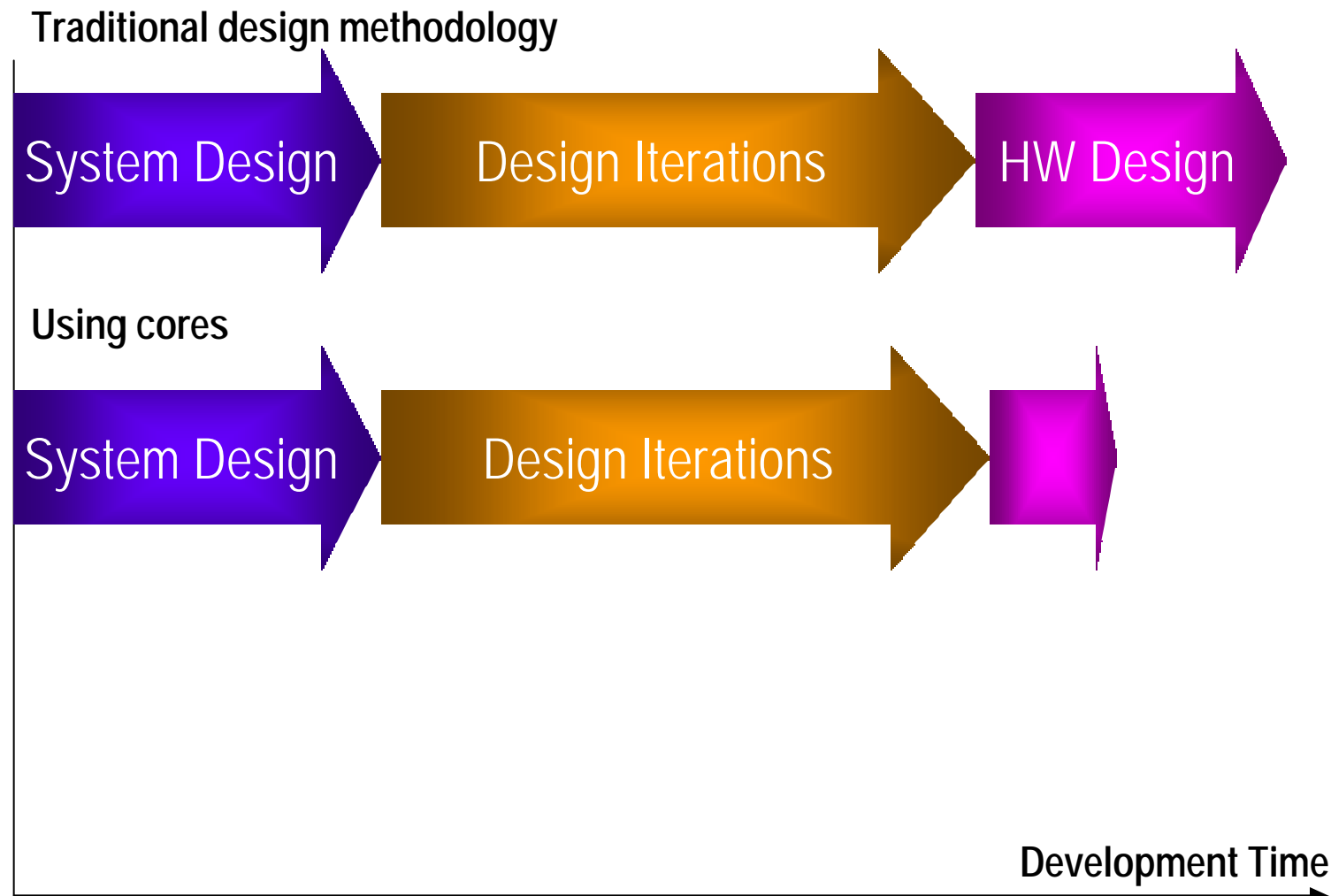
Development Time

New Design Cycle Paradigm

Traditional design methodology

System Design → Design Iterations → HW Design →

Using cores

System Design → Design Iterations →

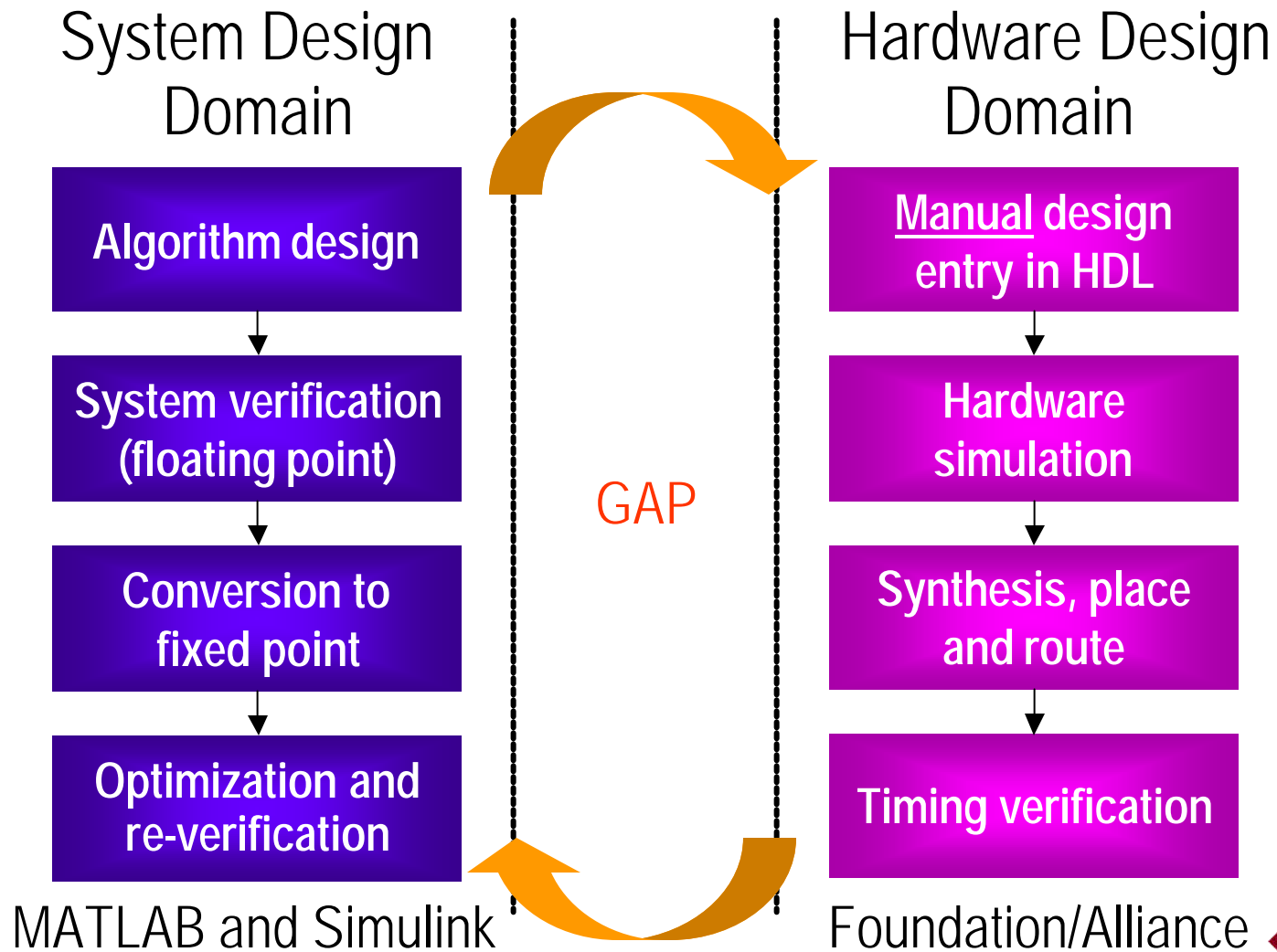**Using The Xilinx SYSTEM Generator for The MathWorks Simulink**

System Design →
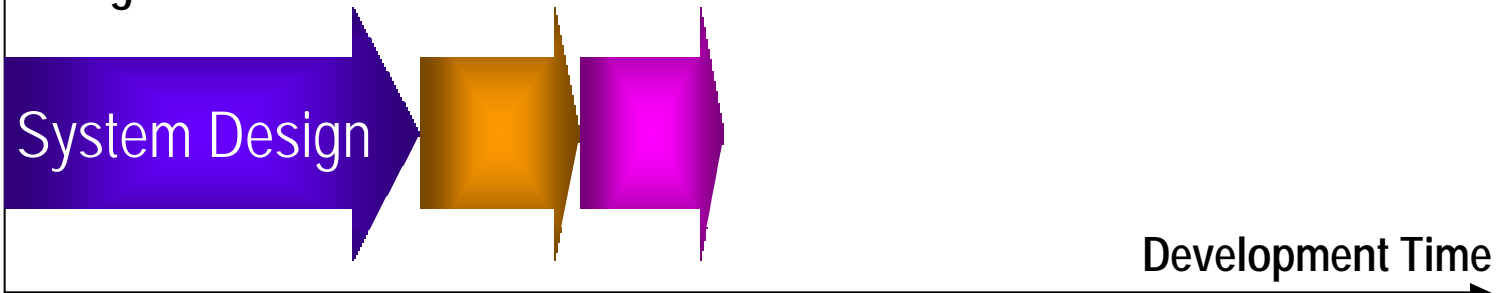
Development Time →

Conclusion

◆New paradigm significantly reduces development time

◆Beat time to market constraints

◆Get passport stamped and sign up to win the "World"

◆Visit the demo stations

The Xilinx SYSTEM Generator for The MathWorks Simulink

Current Gap Between System Design and HW Design

System Design Domain

Algorithm design

↓

System verification (floating point)

↓

Conversion to fixed point

↓

Optimization and re-verification

MATLAB and Simulink

GAP

Hardware Design Domain

Manual design entry in HDL

↓

Hardware simulation

↓

Synthesis, place and route

↓

Timing verification

Foundation/Alliance

The Xilinx SYSTEM Generator for The MathWorks Simulink

System Design Domain

Hardware Design Domain

Algorithm design

System verification (floating point)

Conversion to fixed point

Optimization and re-verification

The Xilinx SYSTEM Generator

Automatic generation of HDL

Hardware simulation

Synthesis, place and route

Timing verification

MATLAB and Simulink

Foundation/Alliance

The MATH WORKS Inc.

XILINX ®

The Xilinx SYSTEM Generator Benefits

- ◆ Optimized implementation including LogiCOREs
  - — Minimal FPGA expertise required

- ◆ Single representations of the design
  - — Less risk for errors – higher quality

- ◆ Significantly reduced development time