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Traditional CPLDs

- CPLDs migrated from Bipolar to CMOS
 - Easier platform to design upon
 - Lower power consumption
 - Continued to use the same Bipolar design technique to implement Product Terms
- Product Term Construction



This technique involves building up a word line using 'wired nor' inputs to a node. As more of these inputs are attached to the node, the capacitance increases and so does the time constant. In order to speed up propagation time, this node is followed by a sense amplifier, which examines the node for approximately a 100mV change to indicate a logic level transition.

Consequences of Using Sense Amplifiers

Power Consumption

- Sense amplifiers are linear elements which always draw a substantial amount of current
- Each sense amplifier consumes 250uA during standby
 - 128 Macrocell device: 160mA of standby current (128MC * 5PTs/MC * 250uA/PT)
- Dynamic power increases as frequency increases

Power Down Modes

- These modes reduce power consumption and performance
- Complicate timing model (additional delays depending on power down level)
- Are often associated with "wake-up" modes which have to be designed around

• Performance

— Performance versus Power Consumption trade-off

Device Size Limitations

Power consumption limits the size of the device you can build

Noise immunity

— Sense amplifier makes the device more susceptible to noise



CoolRunner CPLDs

- New Innovative approach
 - Eliminated Sense amplifiers
 - Removed <u>Performance</u> vs. <u>Power Consumption</u> trade-off
 - Simultaneously deliver high performance and low power consumption
- Product Term Construction



This patented approach is called Fast Zero Power (FZP[™]), and product term word lines are implemented without the use of sense amplifiers. This FZP technology actually uses a CMOS chain of gates to implement product terms. This implementation offers the benefit of much lower power consumption.



CoolRunner Product Term Generation



Consequences of Using FZP

Power consumption

- 1000 times less standby current
- 33% to 50% the total device power consumption
- Simultaneously delivers high performance and low power consumption
- Allows for tremendous amounts of logic resources to be placed in very small packages

Power Down modes

- No power down modes needed
- FZP simultaneously delivers high performance and low power consumption

Performance

- No tradeoffs between performance and power consumption
- Device size /Speed tradeoffs
 - No speed tradeoff for larger devices high speed and low power even at 384 macrocells
- Noise immunity
 - Better noise immunity than sense amp based CPLDs



Technology Difference Summary



Sense Amplifier .25mA each - <u>Standby</u> Higher ICC at Fmax

- Competitive CPLDs bipolar sense amp product terms
 - Always consumes power--even at standby
 - Designer must choose between high performance and low power consumption
 - Limits maximum device size due to power consumption



FZP: CMOS Everywhere - Zero Static Power



- CoolRunner FZP design uses TotalCMOS for product terms
 - Virtually no standby current
 - Dynamic currents 1/3 the competition at F_{max}
 - Simultaneously delivers high performance and low power
 - No power limits on device size



CoolRunner Delivers Lowest Power @ Any Speed



- Reduce lcc requirements while increasing system reliability
 - Smaller power supply
 - Eliminate fans
 - Smaller
 equipment
- Smaller device packaging
 - Less board area
 & more logic
 packing density

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CoolRunner Design Win Examples

- Consumer / Industrial
 - PDA
 - Cell phone
 - MP3 player
 - Battery powered scanner
 - Camcorder iewfinder
 - Digital camera
 - Portable dictation system
 - Gas meter
- High Performance
 - Alpha workstation and server
 - Digital video data link

- Medical
 - Portable syringe pump
 - Home monitoring system
 - Blood analyzer
- PC Peripheral
 - PCMCIA memory card
 - USB based data acquisition
 - Portable computer display
 - White board scanner

