C2910A Microprogram Controller

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Features

- Based on the AMD2910A device
- Pre-defined implementation for predictable timing
- Verified against a hardware model of the original device
- 12-bit data width that addresses up to 4,096 words
- Internal loop counter - pre-settable 12-bit down-counter for repeating instructions and counting loop interactions
- Four address sources
  - Microprogram counter
  - Branch address bus
  - 9-level push/pop stack
  - Internal holding register
- 16 powerful microinstructions
- Output Enable Controls for three branch address sources
- Positive-edge-triggered registers

AllianceCORE™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Documentation
Design File Formats	EDIF Netlist VHDL/Verilog Source RTL available extra
Constraints File	C2910A .ucf
Verification	VHDL/Verilog testbench test vectors
Instantiation Templates	None
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
1076 compliant VHDL simulator, Verilog simulator	
Support	
Support provided by CAST, Inc.	

Applications

The C2910A core is used in high speed bit slice designs.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs[2]	Clock IOBs	IOBs[1]	Performance (MHz)	Xilinx Tools	Special Features
4000XL	4013XL-08	86	1	37	48	M1.5i	None
Spartan	S30-4	87	1	37	40	M1.5i	None
Virtex	V50-6	93[3]	1	37	63	M1.5i	None

Notes:
1. Assuming all core I/O are routed off-chip.
2. Optimized for speed.
3. Utilization numbers for Virtex are in CLB slices.

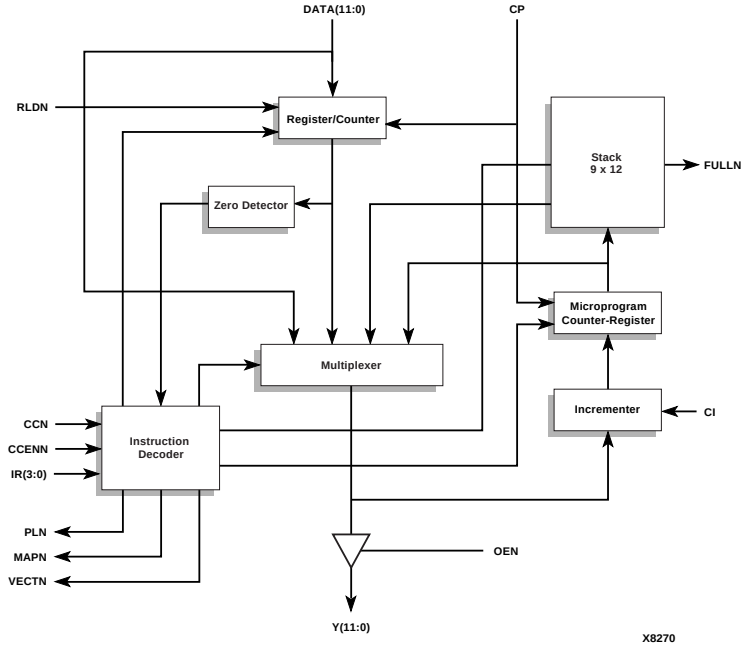

Figure 1: C2910A Microprogram Controller Block Diagram

General Description

The C2910A microprogram controller core is an address sequencer that controls the sequence of execution for the microinstructions stored in microprogram memory. The core can sequentially access the microinstructions, and it provides conditional branching to any microinstructions within the 4,096-microword range. In addition, a 12-bit 9-deep LIFO stack provides a microsubroutine return linkage and looping capability.

Functional Description

The C2910A core is partitioned into modules as shown in Figure 1 and described below. A netlist is provided for the core.

Multiplexer

The four-input multiplexer is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

Register/Counter

This block consists of 12 D-type, edge-triggered flip-flops. When its load control, RLDN is low, DATA is loaded on a positive clock transition. When RLDN is high, the register/counter executes one of the following commands determined by the Instruction Decoder: decrement, hold or load. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address.

Zero Detector

This block signals the Instruction Decoder when the Register/Counter is zero.

Microcontroller Counter/Register (μPC)

This block consists of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 → μPC). Sequential microinstructions are thus executed. When the carry-in is low, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle (Y → μPC). The same microinstruction is thus executed any number of times.

Stack

This 9-word by 12-bit stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer which always points to the last word written. This allows stack reference operations (looping) to be performed without a pop.

Instruction Decoder

This block decodes the incoming instruction and generates the appropriate control signals for all the other blocks. The instruction decoder block also generates the outputs PLN, MAPN, and VECTN.

Core Modifications

The C2910A core can easily be customized to include:

- Larger data width
- Different stack depth

Please contact CAST, Inc. directly for any required modifications.

Pinout

The pinout of the C2910A core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

Core Assumptions

Stack PUSH

After a depth of 9 is reached, the stack is full and the FULLN output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack (9) will be over-written.

It has been observed that the AM2910A device inconsistently destroys the top 2 locations of the stack (8 and 9). This functionality is apparently not documented, and should not be relied upon.

Stack POP

Further POPs from an empty stack will place the bottom data on the Y-Bus (no changes). It has been observed that the AM2910A device will place random data in the Y-Bus during POPs from an empty stack.

To achieve proper result, do not exercise the stack beyond its range (i.e. no PUSHes while the stack is full and no POPs while stack is empty).

Verification Methods

The C2910A Microprogram Controller core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original AM2910A chip, and the results compared with the core's simulation outputs.The C2910A core has also been successfully implemented into silicon.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
RLDN	Input	Register Load Enable
CCN	Input	Condition Code
CCENN	Input	Condition Code Enable
IR (3:0)	Input	Instruction
PLN	Output	Pipeline Address Enable
MAPN	Output	Map Address Enable
VECTN	Output	Vector Address Enable
DATA (11:0)	Input	Direct Data
Y (11:0)	Output	Microprogram Address
OEN	Input	Output Enable
CP	Input	Clock
FULLN	Output	Full Flag
CI	Input	Carry-In

Ordering Information

This product is available from CAST, Inc. Please contact CAST for pricing and more information.

Related Information

Bipolar Microprocessor Logic and Interface Data Book

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