C8254 Programmable Interval Timer/ Counter

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Features

- Supports Virtex™, Virtex-E, and Spartan™-II devices
- Status Read-back Command
- Counter Latch Command
- Read/Write LSB or MSB only; or LSB first, then MSB
- Six Programmable Counter Modes:
  - Interrupt on Terminal Count
  - Hardware Retriggerable One-shot
  - Rate Generator
  - Square Wave Model
  - Software Triggered Strobe
  - Hardware Triggered Strobe (Retriggerable)
- Binary or BCD Counting
- Functionality based on the Intel 8254

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AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Design document
Design File Formats	EDIF, XNF Netlist VHDL Source RTL available extra
Constraints File	C8254.ucf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	VHDL/ Verilog behavioral model
Simulation Tool Used	
1076-compliant VHDL simulator, Verilog simulator	
Support	
Support provided by CAST, Inc.	

Applications

The C8254 core is used in event counter, elapsed-time indicator, programmable one-shot, and in many other designs.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (MHz)	Xilinx Tools	Special Features
Virtex	V100-6	449	4	27	51	3.2i	None
Virtex-E	V100E-8	449	4	27	66	3.2i	None
Spartan-II	2S100-6	449	4	27	48	3.2i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip

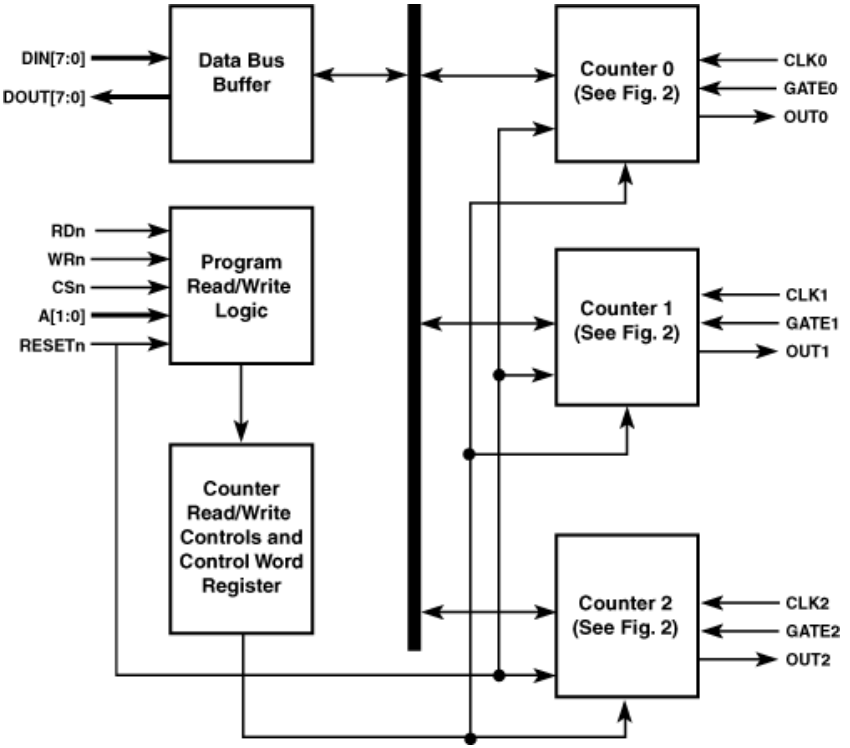

Figure 1: C8254 Programmable Interval Timer/Counter

General Description

The C8254 programmable interval timer/counter core is a high-performance device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters; each counter may operate in a different mode. All modes are software programmable using a CPU.

Functional Description

The C8254 core is partitioned into modules as shown in Figure 1. The internal structure of the counter is shown in Figure 2.

Data Bus Buffer

These input and output 8-bit buffers interface the C8254 to the system Data Bus.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus, then generates control signals for the other functional blocks of the C8254. A1 and A0 select one of the three counters or the Control Word Register, or the read-from or written-into function to the Control Word Register. A low on RDn indicates that the CPU is reading one of the counters; whereas, a low on the WRn indicates that the CPU is writing either a control word or an initial count. Both of these signals are qualified by CSn and are ignored unless the C8254 has been selected by holding CSn low.

Control Word Register

The Control Word is the register which contains the programming of the C8254. It is selected by the Read/Write Logic when A[1:0] = 11. During writing, the data is stored in the Control Word Register and it is interpreted as a control word used to define the operation of the counters.

Control Word Format:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1	SC0	
0	0	Select Counter 0
1	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-back Command

RW1	RW2	
0	0	Counter Latch Command
0	1	Read/Write LSB only
1	0	Read/Write MSB only
1	1	Read/Write LSB first, then MSB

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD	
0	Binary Counter 16-bit
1	BCD Counter (4 decades)

Counter 0, Counter 1, Counter 2

Although each counter is fully independent and may operate in a different mode, they are identical in operation. The following counter description applies to all the counters.

Control Logic

This block controls the 16-bit counter for all counting modes and the Null flag of the counter.

Upper/Lower Byte Controller

The width of the data bus is 8 bits and the counter is 16 bits. The Upper/Lower Byte Controller allows one 8-bit Counter Register, MSB or LSB to be loaded at a time from the internal bus. If the counter is programmed for two-byte read/write mode, this block will control which data will be read at the next read cycle.

Counter Registers

There are two 8-bit registers call CRM and CRL. Both are normally referred to as one unit called CR. When a new count is written to the counter, the count is stored in the CR, then later transferred to the CE16. See Fig. 2. At the rising-edge or WRn, it will write data to the register. One register at a time will be allowed to be loaded from the internal bus. After both registers have been loaded, both bytes are transferred to the CE16 simultaneously. CRM and CRL are cleared when the counter is programmed. Note that the CE16 cannot be written into; whenever a count is written, it is written into the CR.

16-bit Counter

This block contains a 16-bit binary or BCD presettable synchronous down counter.

8-bit Status Register

The 8-bit Status Register contains the Control Word Register, the status of the output and null count flag. When there is a Read-Back command with STATUSn bit enabled and its counter selected, it will latch present status information into Status Register. The status format is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
Out	Null	RW1	RW0	M2	M1	M0	BCD

Bits D5 through D0 contain the counter's programmed mode. Output bit K7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software. Null Count bit D6 indicates when the last count written to the counter register has been loaded into the counting element (CE16). The exact time this happens depends on the mode of the counter.

Read Counter Controller

If both the counter and status of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads returns the latched count (depending on whether the counter is programmed for one or two byte counts). Subsequent reads return the unlatched count. If the counter is programmed for two-byte counts, it will read the LSB first, then the MSB at the next read cycle.

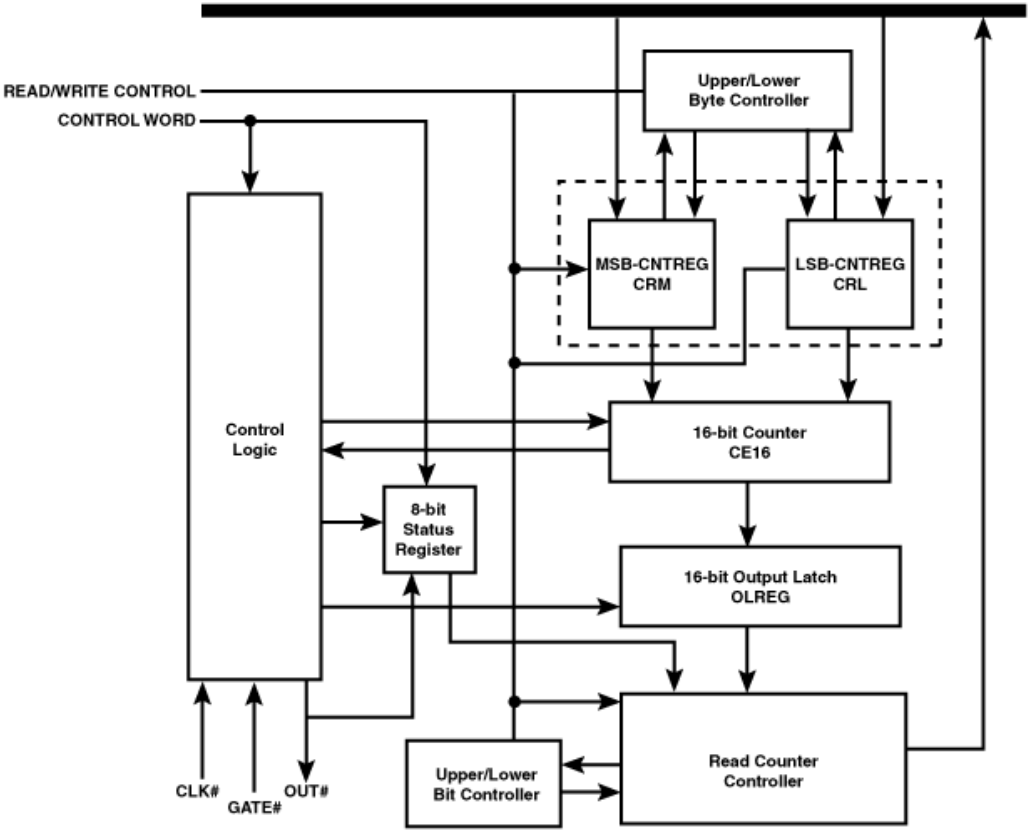

Figure 2: Counter Block Diagram

Core Modifications

The C8254 core can easily be customized to include additional counters.

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C8254 core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
DIN[7:0]	Input	Input Data Bus
DOUT[7:0]	Output	Output Data Bus
RDn	Input	Read Control
WRn	Input	Write Control
CSn	Input	Chip Select
A[1:0]	Input	Address
RESETn	Input	Reset Internal Registers
CLK0	Input	Counter 0 Clock Input
GATE0	Input	Counter 0 Gate Input
OUT0	Output	Counter 0 Output
CLK1	Input	Counter 1 Clock Input
GATE1	Input	Counter 1 Gate Input
OUT1	Output	Counter 1 Output
CLK2	Input	Counter 2 Clock Input
GATE2	Input	Counter 2 Gate Input
OUT2	Output	Counter 2 Output

Core Assumptions

During programming the counter outputs are undefined. The C8254 will stop counting while the counter is being programmed, or during a write word until it loads the initial count from the counter register to the counting element (CE16). If there is a read cycle after the programming, it will read the last counter output data before the start of the programming.

Verification Methods

The functionality of the C8254 core was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Intel 82C54 chip, and the results compared with the simulation outputs of the core.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from CAST Inc. Please contact CAST Inc. directly for pricing and more information.

Related Information

Bipolar Microprocessor Logic and Interface Data Book

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