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Features

- 8-Bit Control Unit
- 8-Bit Arithmetic Logic Unit
- 32-bit Input/Output ports
- Three 16-bit Timer/Counters
- Two Serial Peripheral Interfaces in full duplex mode
- 27-bit Programmable Watchdog Timer
- Three priority Interrupt Controller
- Internal Data Memory interface can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface can address up to 64K bytes of External Program Memory Space and up to 64K bytes of External Data Memory Space
- Dual Data Pointer
- Variable length MOVX instruction to access fast/slow RAM or peripherals
- Special Function Registers (SFR) interface
- Power Management features
- Power management modes IDLE and STOP
- Early-warning power-fail interrupt
- EMI reduction mode disables ALE

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core specification, Instruction set details, Test set details
Design File Formats	.ngo, EDIF Netlist,VHDL Source RTL available at extra cost
Constraints File	D80530.ucf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Example design, assembler programs
Additional Items	Synthesis and simulation scripts
Simulation Tool Used	
1076-Compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs[1]	Clock IOBs[2]	IOBs	Performance[3] (MHz)	Xilinx Tools	Special Features
Virtex-E	V200E-8	1901	1	143	66	M2.1i	None
Virtex	V200-6	1901	1	143	53	M2.1i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip
3. Optimized with disabled IDLE and STOP modes

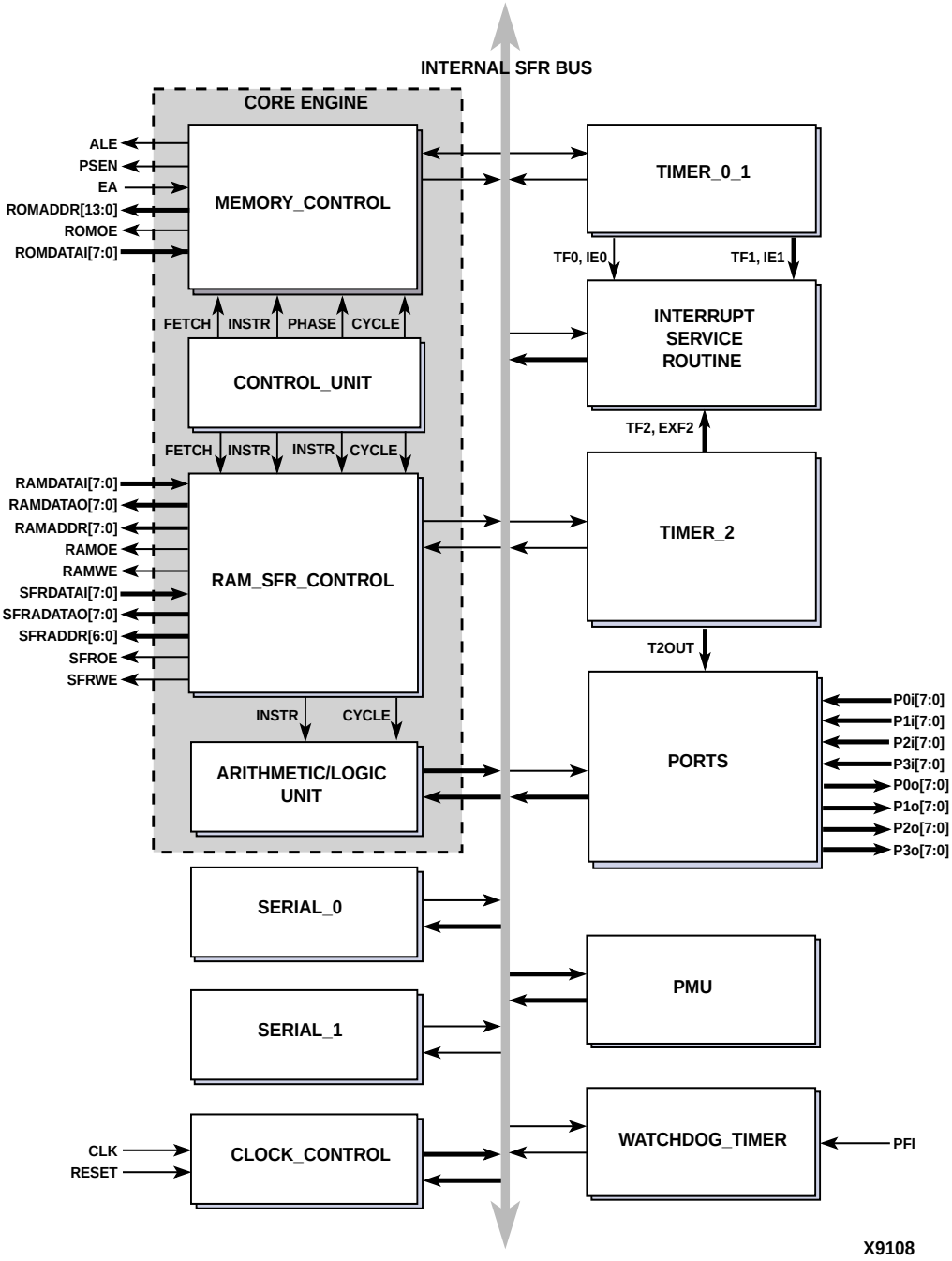

Figure 1: D80530 Microcontroller Block Diagram

General Description

The D80530 is a fast, single-chip, 8-bit microcontroller. It is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C51. The D80530 provides software and hardware interrupts; an interface for serial communications, and a timer system with auto-reload resources.

The D80530 is a microcode-free design and is strictly synchronous with positive-edge clocking, a synchronous reset, and no internal tri-states.

The core architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most instructions have the same number of cycles as bytes. The D80530 uses 4 clocks per cycle. This leads to performance improvement of rate 2.5 (in terms of MIPS) with respect to the legacy 8051 device working at the same clock frequency. The legacy 8051 had a 12-clock architecture.

Table 2 shows the speed advantage of the D80530 over a standard 8051. A speed advantages of 3 means that the D80530 performs the same instruction three times faster than the standard 8051.

Table 2: Core Speed Averages

Speed Advantage	Number Instructions	Number of Op Codes
3	53	160
2	2	2
2.4	16	37
1.5	38	54
1	2	2
Average: 2.5[1]	Sum: 111	Sum: 255

Notes:
1. The actual speed improvement seen in any system will depend on the instruction mix

Functional Description

The D80530 core is partitioned into modules as shown in Figure 1 and described below.

Core Engine

The D80530 core engine is composed of four components:

- Memory control unit
- RAM_SFR control unit
- Control unit
- Arithmetic Logic Unit (ALU)

The D80530 engine allows to fetch instruction from program memory and executes them using RAM or SFR.

Memory Control Unit

- Can address up to 64K bytes of External Program Memory Space
- Can address up to 64K bytes of External Data Memory Space

Control Unit

The Control Unit performs instruction fetch and execution from the Memory Control Unit and the RAM_SFR Control Unit.

RAM SFR Control Unit

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves as Interface for off-core Special Function Registers

Arithmetic Logic Unit (ALU)

The ALU performs:

- 8-bit arithmetic operations
- 8-bit logical operations
- Boolean manipulations
- 8 x 8 bit multiplication
- 8 / 8 bit division

Timer_0_1

This block has two timers: Timer_0 and Timer_1, which are nearly identical. Both have four modes:

- 13-bit Timer/counter
- 16-bit Timer/counter
- 8-bit timer/counter with auto reload
- Two 8-bit timers (Timer_0 only)

Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. The T0 and T1 pins are input through signals of the P3i bus of the Ports block. The user can gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Timer 2

Timer 2 has several capabilities not found in Timers 0 and 1. However, it does not offer the 13-bit and dual 8-bit modes. Thus, it runs in 16-bit mode at all times. Also note that instead of offering the 8-bit auto-reload mode, Timer 2 has a 16-bit auto-reload mode. This mode uses the Timer Capture registers to hold the reload values.

Serial_0 and Serial_1

The D80530 core provides two fully independent serial ports for simultaneous communication over two channels. The serials can operate in identical or different modes and communication speeds. Each serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a

holding register. This allows the serial ports to receive an incoming word before software has read the previous value.

Each port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Interrupt Service Routine

The D80530 core provides a three-priority interrupt system. There are 14 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Ports

The D80530 provides four I/O ports. P0 to P3 are 8-bit bidirectional I/O ports with separated inputs and outputs.

P0 serves as the multiplexed low-order address and data bus during accesses to external program and data memories.

P1 serves the special features, such as, external interrupt inputs, Serial 1 interface, and Timer 2 inputs.

P2 provides the high-order address byte during fetches from external program memory that use 16-bit addresses.

P3 serves the special features, such as, read and write strobes for external data memory, Timer_0 and Timer_1 inputs.

Power Management Unit

The D80530 core has several features related to power consumption and management.

The range of features is shown below

- Power management modes IDLE and STOP
- Early-warning power-fail interrupt
- EMI reduction mode disables ALE

Devices which incorporate the precision voltage reference, have the ability to generate power-fail interrupt. The microcontroller can accept such power-fail interrupt as input. This early warning of supply voltage failure allows time to save critical parameters in nonvolatile memory and put external functions in a safe state.

IDLE mode suspends all engine processing by holding the program counter in a static state. No program values are fetched and no processing occurs. This saves considerable power versus full operation. All clocks remain active, so the timers, Watchdog, and Serial Port functions are all working. Since all clocks are running, the engine can exit the IDLE mode using any of the interrupt sources. There are two ways to exit the IDLE mode. First, any enabled interrupt will cause an exit. The IDLE mode can also be removed using a reset.

STOP mode is the lowest power state that the D80530 core can enter. This is achieved by stopping all on-core clocks, resulting in a fully static condition. No processing is possible, timers are stopped, and no serial communication is possible. Processor operation will halt on the instruction that sets the STOP bit. The STOP mode can be exited in two ways. One method is to use a non-clocked interrupt such as the external interrupt or power-fail interrupt. A second method of exiting STOP mode is with a external reset.

Toggling of ALE causes electromagnetic interference (EMI) noise in typical 8051-based systems. The D80530 core allows for ALE to be disabled in the EMI reduction mode.

Clock Control

This unit generates the internal synchronous reset signal. It also contains registers for selecting the clock for the timers and for programming the length of the external data memory accesses.

Watchdog Timer

The Watchdog Timer is a user programmable clock counter that can serve as a time-base generator, an event timer, or a system supervisor. The timer is driven by the main system clock that is supplied to a series of dividers. The watchdog counter has 27-bit width. The divider output is selectable, and determines the interval between time-outs. When a time-out is reached, an interrupt flag will be set, and if enabled, a reset will occur. The interrupt flag will cause an interrupt to occur if its individual enable bit is set and the global interrupt enable is set.

Core Modifications

The D80530 core can be modified to include features such as:

- 32-Bit Fast Multiplication-Division Unit
- 4x16 Bit Compare/Capture Unit
- 15 bit Programmable Watchdog Timer
- Real Time Clock

Please contact CAST, Inc. directly for any required modifications.

Pinout

The pinout of the D80530 core has not been fixed to specific FPGA I/O, thereby, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1 and described in Table 3.

Verification Methods

The functionality of the D80530 core was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 and Dallas DS80C320 chips, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology, as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

The D80530 core is licensed from Evatronix S.A.

Table 3: Core Signal Pinout

Signal	Signal Direction	Description
Internal Program Memory Interface		
ALE	Output	Address Latch Enable
PSEN	Output	Program Store Enable
EA	Input	External Access Enable
ROMADDR[13:0]	Output	Memory Address
ROMOE	Output	Memory Output Enable
ROMDATAI[7:0]	Output	Memory Bus Output
Internal Data Memory Interface		
RAMDATAI[7:0]	Input	RAM Data Bus Input
RAMDATAO[7:0]	Output	RAM Data Bus Output
RAMADDR[7:0]	Output	RAM Address Bus
RAMOE	Output	Data Output Enable
RAMWE	Output	Data Write Enable
External SFR Interface		
SFRDATAI[7:0]	Input	SFR Data Bus Input
SFRDATAO[7:0]	Output	SFR Data Bus Output
SFRADDR[6:0]	Output	SFR Address Bus
SFROE	Output	SFR Output Enable
SFRWE	Output	SFR Write Enable
Clock_Control		
CLK	Input	Clock
RESET	Input	Chip Reset Input
Interrupt Service Routine		
PFI	Input	Power Fail Interrupt
Ports		
P0i[7:0]	Input	Port 0 Input Bus
P1i[7:0]	Input	Port 1 Input Bus
P2i[7:0]	Input	Port 2 Input Bus
P3i[7:0]	Input	Port 3 Input Bus
P0o[7:0]	Output	Port 0 Output Bus
P1o[7:0]	Output	Port 1 Output Bus
P2oi[7:0]	Output	Port 2 Output Bus
P3o[7:0]	Output	Port 3 Output Bus

Related Information

- *High-Speed Microcontroller Data Book*, Dallas Semiconductor, 1995.
- *CMOS Single-chip 8-bit Micro controllers*, Philips, 1996.
- *Addendum to the MCS®51 Microcontroller Family*, Intel, 1996.
- *8-bit Embedded Controllers*, Intel, 1990

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