CAST

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Features

- Supports Spartan™-II, Virtex™, and Virtex™-E devices
- Formats data as per X.25 (CCITT) level-2 standards
- Single byte address recognition
- 16 -bit and 32-bit frame check sequence (CRC)
- High speed serially clocked output. The data rate is equal to the clock rate
- Motorola M6800 microprocessor interface
- Software reset
- Supports multiplexing multiple HDLCs
- Internal registers for buffering

Applications

- Data link controllers and protocol generators
- Digital sets, PBXs, and private packet networks
- D-channel controller for ISDN basic access

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AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex
Device Tested	V50-6
CLB Slices	210
Clock IOBs	2
IOBs	26
Performance (MHz)	60
Xilinx Core Tools	M1.5i
Special Features	None
Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF Netlist VHDL, RTL available extra
Constraints File	hdlc.ucf
Verification Tool	VHDL testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	None
Simulation Tool Used	
1076 Compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Notes:
1. Assuming all core I/Os are routed off-chip.

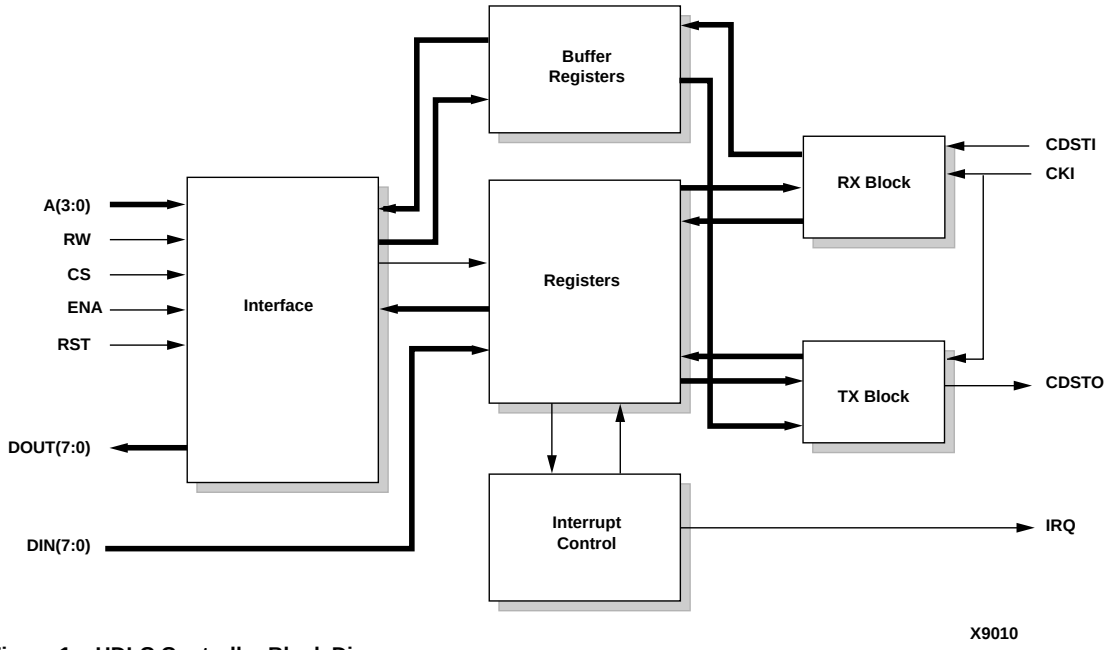

Figure 1: HDLC Controller Block Diagram

General Description

The HDLC Controller handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (Level 2) recommendations of the CCITT. It transmits and receives the packeted data (information or control) serially as shown in Figure 1, while providing the data transparency by zero insertion and deletion. It generates and detects flags that indicate the status of HDLC. Further, it provides 16- or 32- bit cyclic redundancy check on data packets using the CCITT defined polynomial. It also recognizes a single byte address in the received frame.

Functional Description

The HDLC core is partitioned into modules as shown in figure 1 and described below:

Interface

This module handles the reading and writing actions of the M6800 microprocessor.

Buffer Registers

This block consists of receiver & transmitter buffer registers that store data obtained from the RX block and also data to be sent to the TX block.

Registers

Includes all the microprocessor controllable registers.

Interrupt Control

Interrupt control logic handles all the interrupts and records them in the interrupt flag register.

RX block

Receives the serial data, and stores it to the receiver buffer register.

TX block

Transmits the parallel data from the transmit buffer register to the serial output line TXD.

Core Modifications

The HDLC core can be easily customized, to include:

- Processor interface modified per customer's needs
- Enabling/disabling functions for transmitter and receiver
- Abort sequence

Please contact CAST, Inc. directly for any required modifications.

Pinout

The pinout of the HDLC Controller core has not been fixed to specific FPGA I/O, allowing flexibility with a user's appli-

cation. Signal names are shown in the block diagram in Figure 1, and in Table 2.

Verification Methods

The HDLC Controller core's functionality has been extensively tested with a VHDL testbench and a large number of test patterns.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

The HDLC Controller is available directly from CAST, Inc. Please contact CAST, Inc. for pricing and additional information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

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E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[3:0]	Input	Address bus inputs. Selects internal registers in conjunction with CS, and R/W inputs, and ENA clock.
RW	Input	Read/write control for microcontroller readable/writable registers.
CS	Input	Chip select. Active LOW chip select to enable read or write operations to the registers in the HDLC.
ENA	Input	Enable clock. Activates the address bus and R/W input and enables data transfers on the data bus.
RST	Input	Reset input. Active LOW reset input which resets all the registers.
DOUT[7:0]	Output	Microprocessor output data bus. Allows the data transfer from the HDLC controller to the microprocessor.
DIN[7:0]	Input	Microprocessor input data bus. Allows the data transfer from the microprocessor to the HDLC controller.
CDSTI	Input	The serial data input line.
CKI	Input	Clock input. Bit Rate clock in the External Timing Mode. It is used for shifting the formatted packets in and out.
CDSTO	Output	The serial data output line.
IRQ	Output	Interrupt request output.