CoreEl MicroSystems

CoreEl MicroSystems

4046 Clipper Court
Fremont, CA 94538 USA
Phone: +1 510-770-2277
Fax: +1 510-770-2288
URL: www.coreel.com
E-mail: sales@coreel.com

Features

- Pre-defined implementation for predictable timing in Xilinx FPGA or HardWire[a]
- Octet-wide operation
- State Machine
  - Hunt, Presync, and Sync states
  - Correction and Detection states within the Sync state
- Loss of cell delineation indication
- Idle cell discard
- The header of an input cell, after any error correction, is compared with the header contents specified in ATM UNI 3.1 for an idle cell; such detected idle cells are discarded by disabling the output_enable signal.
- HEC Verification
  - Coset polynomial added before verification
  - Single bit error correction, multiple bit error detection
  - Indication upon an uncorrectable error (cell discard)
- Cell Descrambling
  - Always descrambles cell payload
  - Self synchronizing scrambler-descrambler process specified in ATM UNI 3.1
- Cell received pulse output
- Cell discarded pulse output
- Continuous clock with cycle-by-cycle enable

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000XL	
CLBs Used	270	
IOBs Used	23[1]	
CLKIOBs Used	2	
System Clock f_{max}	40 MHz	
Device Features Used	Global Clock Buffers	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4010XL-09 PC84	38[1]	130
Provided with Core		
Documentation	Product Brief Specification Document Design Document Test Bench Design Document Test Script	
Design File Formats	VHDL compiled, EDIF netlist	
Constraint Files	UCF File, Exemplar scripts	
Verification Tool	Script Based behavioral VHDL Test Bench	
Schematic Symbols	None	
Evaluation Model	Behavioral VHDL	
Reference Designs and Application Notes	ATM-UNI Specifications	
Additional Items	ITU-T I.432 Specifications	
Design Tool Requirements		
Xilinx Core Tools	M1.3.7 or later	
Entry/Verification Tool	Model Tech V-System	
Support		
Support provided by CoreEl Microsystems		

Note:
1. Assuming all core signals are routed off-chip.

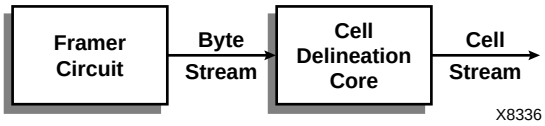

Figure 1: Typical Application of Cell Delineation Core

Applications

The Cell Delineation core can be used in Asynchronous Transfer Mode (ATM) networking systems such as adapter cards, routers and switches.

General Description

The Cell Delineation core (CC-200) carries out the functions required in the receive stream of the Transmission Convergence sub-layer of an ATM Physical Layer processor (see Figure 1). The input is a byte-aligned cell stream containing 53-byte cells with 5 bytes of header and 48 bytes of payload. CC-200 delineates cells as prescribed in ITU specification I.432 and gives out header and payload.

Functional Description

The Cell Delineation core is divided into eight blocks as shown in Figure 2: Data Buffer, HEC Computation Module, Correction Mask Generator, Cell Delineation State Machine, Byte Counters, Idle Cell Detect Logic, Controller and Descrambler.

Block Descriptions

The clock, clockenable and reset_b signals are common to all blocks. The input data is passed through a nine-byte wide buffer and data at five particular buffer positions as indicated in Figure 2, and is fed to the Idle Cell Detect Logic block, to determine whether the cell is assigned or idle.

The HEC computation module checks whether the HEC computed over the first four header bytes matches with the data in the fifth byte and indicates it using HECError signal. It uses the polynomial specified in ATM UNI 3.1.

Cell delineation is carried out by the Cell Delineation State Machine and the Controller block which controls the mechanism.

The Byte Counter keeps track of the number of bytes in a cell (53). It is reset using Reset_cntr signal as well, which is

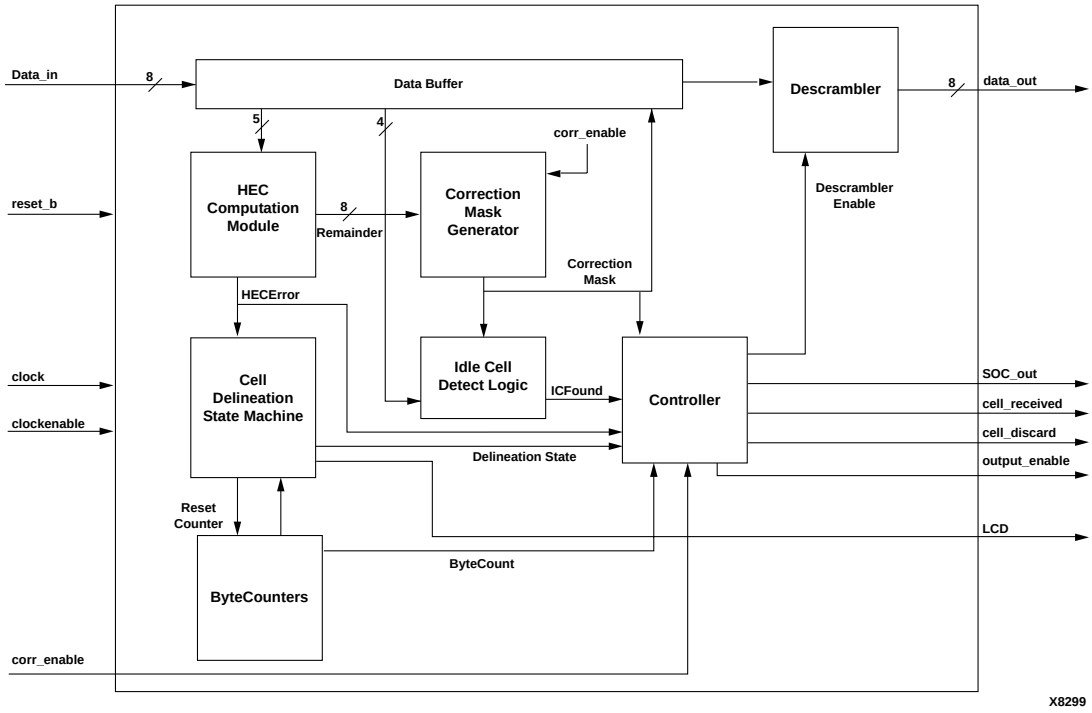

Figure 2: Cell Delineation Core Block Diagram

generated by the Cell Delineation State Machine. The Byte Counter outputs the byte count to the Controller block and the expected location of the header to the Cell Delineation State Machine.

The correction mask generator block takes the remainder from the HEC computation module and finds out the correction mask required in order to correct a single bit error in the header.

The descrambler module descrambles only payload octets using the polynomial specified in ATM UNI 3.1. It descrambles the cell payload using the self-synchronizing scrambler procedure specified in ATM UNI 3.1. When an input cell header matches the pattern specified for idle cells, the cell is discarded.

Basic Operation

In the initial Hunt state, the core performs a byte-by-byte search for possible header locations by applying the CRC check specified by the ATM Forum.

Upon detection of a possible valid header, the state machine enters the Presync state where it verifies the validity of the current cell delineation by checking the CRC Header Error Check (HEC) sequence recorded in the 5th byte of each cell. Upon a successful match for 6 consecutive cells, the state machine enters the Sync state in which cell streams are given out along with a Start-of-cell indication.

The Sync state consists of two sub-states called Correction and Detection. In the Correction state, an attempt is made to correct a cell header with a single bit error. Detection of a multiple bit error results in the cell being discarded. In either case the Detection state is entered where no attempt is made to correct any cell header.

8 consecutive cells with correct header patterns would take the state machine back to the Correction state. Seven consecutive incorrect header patterns would take the state machine back to the Hunt state.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEl can perform special modifications for additional charge. However source code is available for additional cost where the customer can make modifications. Contact CoreEl Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for the core are provided in the block diagram shown in Figure 1, and described in Table 1.

Table 1: Signal Core Pinout

Signal	Signal Direction	Description
data_in(7:0)	Input	Byte aligned input carrying a continuous stream of 53-byte cells.
reset_b	Input	Asynchronous reset; active low.
clock	Input	Clock of up to 80 MHz compatible with E3, STS-3c, and STS-12c applications; uses 1 FPGA CLKIOB pin.
clockenable	Input	Indicates clock cycles during which module is active; uses 1 FPGA CLKIOB pin.
corr_enable	Input	Command indicating attempt to correct single bit errors in cell header; active high.
data_out(8:0)	Output	Output data containing 52-byte cells - 4 bytes header and 48 bytes payload.
SOC_out	Output	Start of cell indication; active high.
cell_received	Output	Indicates complete reception of a cell; active high. One clock wide pulse.
cell_discard	Output	Indicates cell has been discarded due to header error; active high. One clock wide pulse.
output_enable	Output	Indicates data on output bus is valid in current clock cycle; active high.
LCD	Output	Indicates loss of cell delineation; active high.

Verification Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a Model technology V-System environment.

The test bench was written in VHDL with very powerful scripting capabilities and several scripts have been written for verifying the implementation. Additional tests can be added to the testbench by writing new scripts.

Recommended Design Experience

Knowledge of ATM technology and ATM Forum specifications is needed. User should be familiar with HDL design methodology including FPGA targeting. Using the test-

bench requires familiarity with V-System of Model Technology.

Available Support Products

CoreEl offers a test bench for verifying the core along with a complete line of ATM Core Cells for Xilinx FPGAs that perform the following functions:

- UTOPIA Slave Interface
- Cell Delineation
- CRC-32
- CRC-10

Ordering Information

For information on this or other products mentioned in this specification, contact CoreEl Microsystems directly from the information provided on the front page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

ATM Forum
Worldwide Headquarters
2570 West El Camino Real, Suite 304
Mountain View, CA 94040-1313
Tel: +1 650-949-6700
Fax: +1 650-949-6705
E-mail: info@atmforum.com
URL: www.atmforum.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)