CSELT S.p.A

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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Noisy transmission channel emulator
- Field programmable noise generation profile
- Customizable VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module
- Core customization:
  - Number of channel input bits
  - Number of channel output bits per channel input bit (allows emulation of a quantizer at the channel output)
  - Parallel programming data bus width
  - Pseudo Random Generator (LFSR) definition parameters: LFSR size, LFSR feedback polynomial, LFSR seed (reset value)

Applications

- Emulation of a noisy transmission channel

AllianceCORE™ Facts

Core Specifics[1]		
Supported Family	Spartan	Virtex
Device Tested	S40-3	V50-6
CLBs[2]	261	173
Clock IOBs	1	1
IOBs[3]	46	46
Performance (MHz)	39	100
Xilinx Tools	M1.5i/M2.1i	M1.5i/M2.1i
Special Features	None	None

Provided with Core	
Documentation	User Manual
Design File Formats	EDIF netlist, XNF netlist, VHDL source available extra
Constraints File	TOP_channel_nl.ncf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	None

Simulation Tool Used
Synopsys VSS

Support
Design and customization support provided by CSELT

Notes:
1. Data refer to the following customization:
   - 3 quantization bits
   - 2 channel input bits
   - 8 programming data input bits
   - 24-bit pseudo random generator with polynomial $(1C20008)_{16}$ and seed $(557074)_{16}$
2. Utilization numbers for Virtex are in CLB slices
3. Assuming all core I/Os are routed off-chip

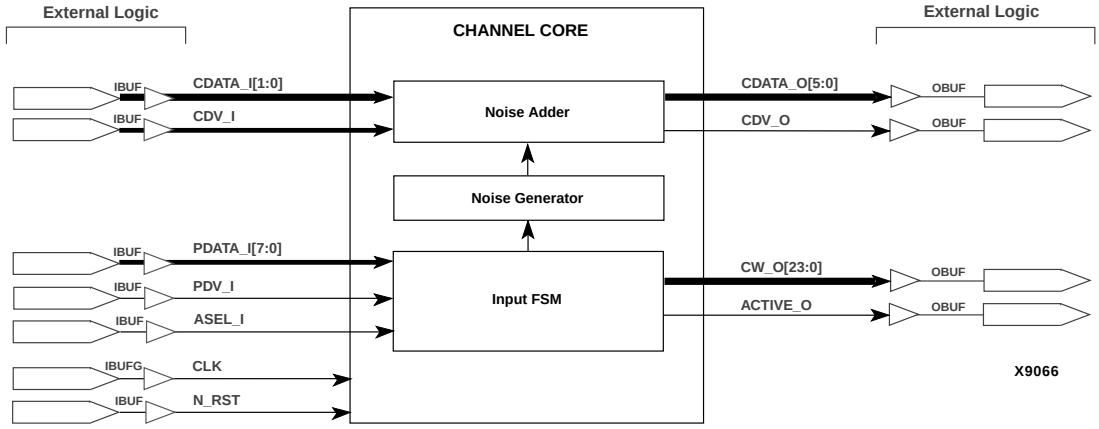

Figure 1: Channel Block Diagram

General Description

The Channel core implements a noisy transmission channel model, useful for hardware emulation.

User customizable core features include the channel symbol size (i.e. the number of channel input bits) and the number of channel output bits per input bit (used for specifying the number of output quantization levels).

The channel noise is produced by a pseudo random generator, implemented as a linear feedback shift register (LFSR). The LFSR value v is compared against a set of n-1 thresholds, $T_1 \ldots T_{n-1}$, where n is the number of output quantization levels. If $T_i < v < T_{i+1}$, then value of the generated error is i. The error value is then XOR'ed to the input value (expanded to the appropriate number of bits) to generate the channel output.

Threshold values are stored into internal registers, loaded via a parallel port whose size is user-definable. This allows the user to model specific noise levels and profiles, and to change them during the emulation.

The Absolute Maximum ratings, Operating Conditions, DC Electrical Specifications and Capacitances depend on the Xilinx device selected for implementation and can be retrieved from the corresponding Xilinx datasheet.

Functional Description

The internal architecture of the Channel core is shown in Figure 1. A brief description of the operation of each module follows.

Input FSM

The input FSM handles the programming of the threshold values through the PDATA_I parallel port. Since both threshold addressed and data are input through PDATA_I, the ASEL_I input is used to signal the presence of a threshold address on PDATA_I.

Noise Generator

The noise generator module is composed of a pseudo random generator and a set of comparators that compare the pseudo random value against the user-defined thresholds, producing the noise samples. The random generator is a linear feedback shift register (LFSR).

Noise Adder

This module is responsible for adding noise to the data flow, which is serialized before this operation.

Pinout

The pinout of this core has not been fixed to a specific FPGA I/O allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and described in Table 1.

Core Modifications

CSELT provides netlist customized to user's requirements. The Channel core source code is parametric. Parameters shown in Table 2 are implemented as a set of generics in the synthesizable VHDL source code of the core. Parameters allow the user to specify some architectural and functional features so as to customize the netlist to a specific design or application.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
CDATA_I[1:0]	Input	Channel data input; port size is equal to NSB, NSB is a generic
CDV_I	Input	Channel data valid input
PDATA_I[7:0]	Input	Parallel data input; port size equal to DSIZE, DSIZE is a generic
PDV_I	Input	Parallel data valid input
ASEL_I	Input	Address select input
CLK	Input	Master clock
N_RST	Input	Asynchronous reset
CDATA_O[5:0]	Output	Channel data output; port size equal to NSB x NQB (both generic values)
CDV_O	Output	Channel data valid output
CW_O[23:0]	Output	Control word output; port size equal to NRSB (a generic)
ACTIVE_O	Output	Input FSM activity flag

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Table 2: Core Parameters (VHDL Generics)

Parameter	Description
BASEADR	Base address of the threshold register array
DSIZE	Number of bits in a parallel data input word
NQB	Number of bits in a quantizer sample (output bits per input bit)
NSB	Number of bits in a channel symbol (channel input bits)
NRSB	Number of bits in a random sample (LFSR length)
GENPOL0	LFSR feedback polynomial, lowest degree terms
GENPOL1	LFSR feedback polynomial, highest degree terms
SEED0	LFSR seed, lowest degree terms
SEED1	LFSR seed, highest degree terms

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation have been performed for different values of the core parameters, using Synopsys VSS simulator. Simulation scenarios (including data and command files) and parametric testbench, design verification tools, are provided with the core.

The parametric testbench is composed of a data stream generator, a clock/reset generator and a noise threshold programming interface. The input data stream and the noise thresholds of the channel are easily customizable by editing some text files.

Ordering Information

The Channel core is provided under license by CSELT S.p.A. for use in Xilinx programmable logic devices. Please contact CSELT S.p.A for information about pricing, terms and conditions of sale.

CSELT S.p.A reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

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Recommended Design Experience

Experience with Xilinx design flow is recommended to users of netlist version of this core. For the source code version, users should also be familiar with the Synopsys FPGA synthesis tools (VHDL Compiler, FPGA Compiler) and simulator (VSS).

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Channel
Implementation Request Form

To: CSELT S.p.A.

FAX: +39 011 228 7003

E-mail: viplibrary@cselt.it

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

CSELT configures and ships Xilinx netlist versions of the Channel core customized to your specification. Please fill out and fax this form so that CSELT can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

Implementation Issues

1. Number of bits of the threshold bus: _____

2. Number of channel input bits: _____

3. Number of channel output bits per input bit: _____

4. LFSR feedback polynomial:_____

5. LFSR seed (reset value): _____

Business Issues

1. Indicate timescales of requirement:
_____ date for decision
_____ date for placing order
_____ date of delivery

2. Indicate your area of responsibility:
_____ decision maker
_____ budget holder
_____ recommender

3. Has a budget been allocated for the purchase?
Yes _____ No _____

4. What volume do you expect to ship of the product that will use this core? _____

5. What major factors will influence your decision?
_____ cost
_____ customization
_____ testing
_____ implementation size

6. Are you considering any other solutions?