UTOPIA_L2_RX UTOPIA Level 2 PHY Side RX Interface

CSELT S.p.A

Via G. Reiss Romoli, 274
I-10148 Torino, Italy
Phone: +39 011 228 7165
Fax: +39 011 228 7003
E-mail: viplibrary@cselt.it
URL: www.cselt.it

Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Protocol conversion from Pb to UTOPIA level 2, RX mode, PHY side
- Customizable VHDL source code available allowing generation of different netlist versions
- DPRAM based internal buffering for clock decoupling
- Programmable testbench for pre- and post-synthesis verification supplied with the module
- Core customization:
  - 8/16 bits interface data width
  - Cell error detection mode (short cell, long cell)
  - Cell error management mode (no action, flag, discard)
  - Physical idle cell recognition and discard (yes/no)
  - Reset mode (synchronous/asynchronous)
  - Size of the internal buffer memory

Applications

- Physical layer ATM circuits

AllianceCORE™ Facts

Core Specifics[1]		
Supported Family	Spartan	Virtex
Device Tested	S20-3	V50-6
CLBs[2]	222	63
Clock IOBs	2	2
IOBs[3]	37	37
Performance (MHz)	34	53
Xilinx Tools	M1.5i/M2.1i	M1.5i/M2.1i
Special Features	TBUFs, SelectRAM	BlockRAM
Provided with Core		
Documentation		User Manual
Design File Formats		EDIF netlist, XNF netlist, VHDL source available extra
Constraints File		TOP_U2PRX_nl.ncf
Verification		VHDL testbench
Instantiation Templates		VHDL, Verilog
Reference Designs & Application Notes		None
Additional Items		None
Simulation Tool Used		
Synopsys VSS		
Support		
Design and customization support provided by CSELT		

Notes:
1. Data refer to the following customization:
   8-bit interface;
   Data parity, short and long cell error flags;
   Physical idle cell recognition and discard;
   Asynchronous reset; and
   Internal buffer size = 4 ATM cells
2. Utilization numbers for Virtex are in CLB slices
3. Assuming all core I/Os (excluding N_CTSENB and N_TSENB) are routed off-chip

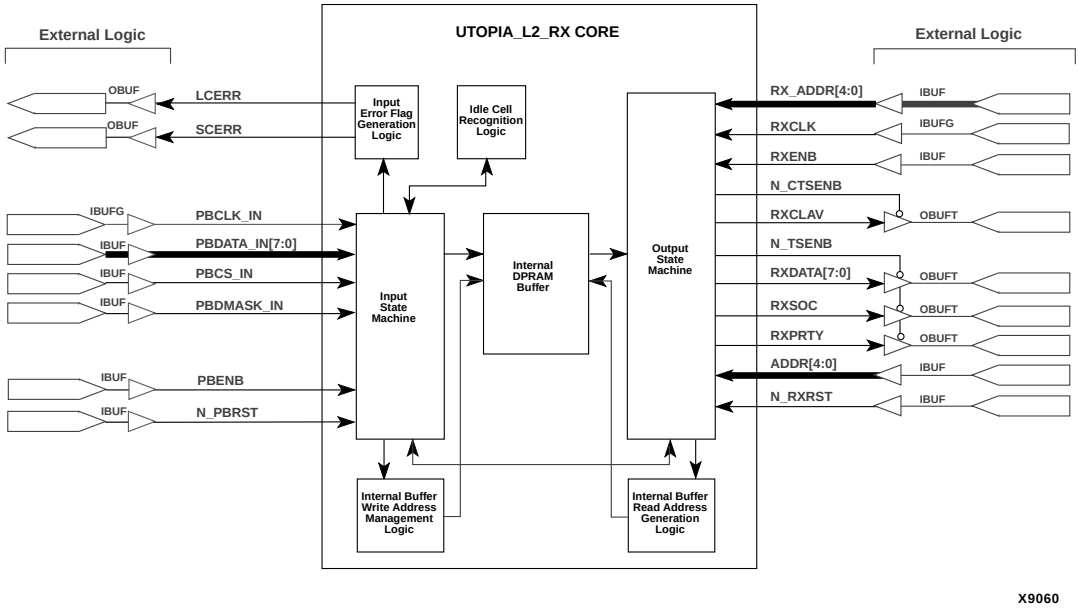

Figure 1: UTOPIA_L2_RX Block Diagram

General Description

The UTOPIA_L2_RX Level 2 Interface core implements an interface between two ATM cell transfer protocols - the Pb protocol (as defined in RACE BLNT) and the ATM Forum UTOPIA level 2 protocol (PHY RX side, cell level). Either the 8 bit or the 16 bit data transmission mode can be implemented, depending on the selected customization.

The core can store a limited amount of ATM cells in a local buffer for clock decoupling purposes. Besides, it can handle cell length errors in accordance with a user customizable error handling mode; three different handling modes (no action, flag, discard) are provided.

The Absolute Maximum ratings, Operating Conditions, DC Electrical Specifications and Capacitances depend on the Xilinx device selected for implementation and can be retrieved in the corresponding Xilinx datasheet.

Functional Description

The internal architecture of the UTOPIA_L2_RX core is shown in Figure 1. A brief description of the operation of each module follows.

Input State Machine

The Input State Machine handles the Pb input interface and the write port of the DPRAM cell buffer. Besides, it performs cell integrity controls and flags or discards faulty cells in accordance with the error handling policy set for the core implementation. Finally, it discards physical idle cells (only if that option has been selected for implementation).

It has to be pointed out that short cells can always be discarded, while sometimes the long cells cannot. The above happens because a received cell becomes available to the output interface as soon as the last valid cell byte/word is received. So, the first extra byte/word of a long cell could be received when the corresponding cell is already being output – or, even, has already been completely output.

Output State Machine

The Output State Machine handles the UTOPIA level 2 PHY RX interface and the read port of the DPRAM cell buffer.

If the short cell discard option is not implemented, short cells are completed with unpredictable data. Long cells are always truncated.

Internal Buffer Write/Read Address Management Logic

The Address Management modules handle the generation of the read and write addresses of the DPRAM cell buffer. The cell buffer is structured as a paged memory; the memory page size is one ATM cell (53 bytes in 8 bit mode, 54 bytes in 16 bit mode). The Address Management modules exchange information about the page being read/written, that is used by the Input and Output State Machines to detect the buffer full and empty status.

Since Write and Read Address Management logic are clocked by different clocks, dual-rank synchronizers are used to decouple the connections between them. Also, the page address counters are implemented as Gray counters to avoid race conditions.

Input Error Flag Generation Logic

The Input Error Flag Generation Logic handles the output of the error flags generated by the input interface. Input error flags are raised as soon as the error condition causing them occurs, and last for one input clock cycle.

Internal DPRAM Buffer

The internal DPRAM buffer is a dual port RAM in which cell data are stored. The actual size of the buffer memory depends on both the device family (DPRAM primitive size is 16 bits for SPARTAN SelectRAM and 4 Kbits for Virtex BlockRAM) and on the value of the NPAGES generic parameter set for the desired implementation.

Idle Cell Recognition Logic

The Idle Cell Recognition Logic is a state machine that recognizes the data corresponding to an idle cell header for the ATM physical layer, as specified in the ITU-T I-432 recommendation. Physical layer idle cells are used to ensure stream continuity in cell based data transmission, and must be removed by the receiver end of the physical link. This module is included in the core only if the physical idle cell recognition and discard option has been selected for implementation.

Pinout

The pinout of this core has not been fixed to a specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and described in Table 1.

Core Modifications

CSELT provides netlist customized to user's requirements. The UTOPIA_L2_RX source code core is parametric. Parameters shown in Table 2 are implemented as a set of generics in the synthesizable VHDL source code of the core. These parameters allow the user to specify some architectural and functional features so as to customize the netlist to a specific design or application.

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation has been performed for different values of the core parameters, using the Synopsys VSS simulator. Simulation scenarios (including data and command files) and parametric test bench used for design verification are provided with the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
UTOPIA Interface		
RXADDR[4:0]	Input	Address bus
RXCLK	Input	Data clock
RXCLAV	Output	Cell available flag; three-state
RXENB	Input	Transmission enable
RXSOC	Output	Start of cell flag, three-state
RXPRTY	Output	Data parity, three-state
RXDATA[7:0]	Output	Data, three-state; port size can be 8/16 bits depending on the DMODE generic
Pb Interface		
PBDATA_IN[7:0]	Input	Data; port size can be 8/16 bits depending on the DMODE generic
PBCS_IN	Input	Start of cell flag
PBDMASK_IN	Input	Data mask
Control and Status Ports		
LCERR	Output	Long cell error flag (Pb interface)
SCERR	Output	Short cell error flag (Pb interface)
PBENB	Input	Pb interface output enable
N_CTSENB	Output	RXCLAV output enable, active low
N_TSENB	Output	RX port output enable, active low
ADDR[4:0]	Input	UTOPIA port address
Clock and Reset Ports		
PBCLK_IN	Input	Pb data clock input
N_PBRST	Input	Reset (PBCLK_IN clocked registers)
N_RXRST	Input	Reset (RXCLK clocked registers)

Table 2: Core Parameters (VHDL Generics)

Parameter	Description
DMODE	Data transfer mode (8/16 bit)
ERRCHECK	Data error check configuration
IDLEGEN	Idle cell recognition/discard mode (active/inactive)
NPAGES	Internal buffer depth (cells)
RSTMODE	Reset mode (synchronous/asynchronous)

The parametric test bench is composed of a programmable ATM cell generator with Pb interface, and of a UTOPIA level 2 RX interface, ATM side. The generator produces a cell stream that is easily customizable through cell generation commands read from a text file. Cell stream customizability includes header data, (random or user-defined), payload data (random, counter, fixed or user-defined), period and size of transmission holes, error injection (data errors, cell length errors).

The UTOPIA RX interface performs polling of the PHY side interface ports, and receives available cells from them. PHY ports are selected for transmission using a round robin algorithm.

Recommended Design Experience

Experience with the Xilinx design flow and ATM transmission system design is recommended to the users of the netlist version of the core. For the source code version, users should also be familiar with the Synopsys FPGA synthesis tools (VHDL Compiler, FPGA Compiler) and simulator (VSS).

Ordering Information

The UTOPIA_L2_RX core is provided under license by CSELT S.p.A for use in Xilinx programmable logic devices. Please contact CSELT S.p.A for information about pricing, terms and conditions of sale.

CSELT S.p.A reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

All trademarks, registered trademarks, or servicemarks are property of their respective owners.

Related Information

A copy of the interface specification is available at the ATM Forum web site:

ftp.atmforum.com/pub/approved-specs/af-phy-0039.000.pdf

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

UTOPIA_L2_RX
Implementation Request Form

To: CSELT S.p.A

FAX: +39 011 228 7003

E-mail: viplibrary@cselt.it

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

CSELT configures and ships Xilinx netlist versions of the UTOPIA_L2_RX core customized to your specification. Please fill out and fax this form so that CSELT can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

Implementation Issues

1. Data transfer mode (8 bit / 16 bit): _____

2. Flag short cells? _____

3. Discard short cells? _____

4. Flag long cells? _____

5. Discard long cells (when possible)? _____

6. Internal buffer depth (cells): _____

7. Idle cell recognition and discard required? _____

8. Reset mode (sync/async): _____

Business Issues

1. Indicate timescales of requirement:
_____ date for decision
_____ date for placing order
_____ date of delivery

2. Indicate your area of responsibility:
_____ decision maker
_____ budget holder
_____ recommender

3. Has a budget been allocated for the purchase?
Yes _____ No _____

4. What volume do you expect to ship of the product that will use this core? _____

5. What major factors will influence your decision?
_____ cost
_____ customization
_____ testing
_____ implementation size

5. Are you considering any other solutions? _____