GV & Associates, Inc.

23540 Oriente Way
Ramona, CA 92065 USA
Phone: +1 760-789-7015
Fax: +1 760-789-7015
E-mail: loop@gvassociates.com
Web: www.gvassociates.com

Features

- 65 MHz maximum input A/D sample rate
- 30 MHz sample Bandwidth
- Each FPGA has access to both A/Ds
- Each FPGA has access to both D/As (via Local Bus)
- FPGA Logic Expansion (20K to 800K gates)
- Two Dedicated 64K X 16 SRAM for each FPGA
- Up to 114,688 bits of internal Block RAM

- Four Delay Locked Loops (DLL)
- 86 bit FPGA Local Bus with External Data Access
- Slave Serial and Download Cable (Model DLC4) Configurable
- 120 MHz maximum output D/A sample rate
- Separate FPGA Power Plane for Power Measurement
- External 2.5V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- On Board 120 MHz Clock Oscillator
- External High Stability Clock Input

General Description

The GVA-250 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx Virtex FPGA family.
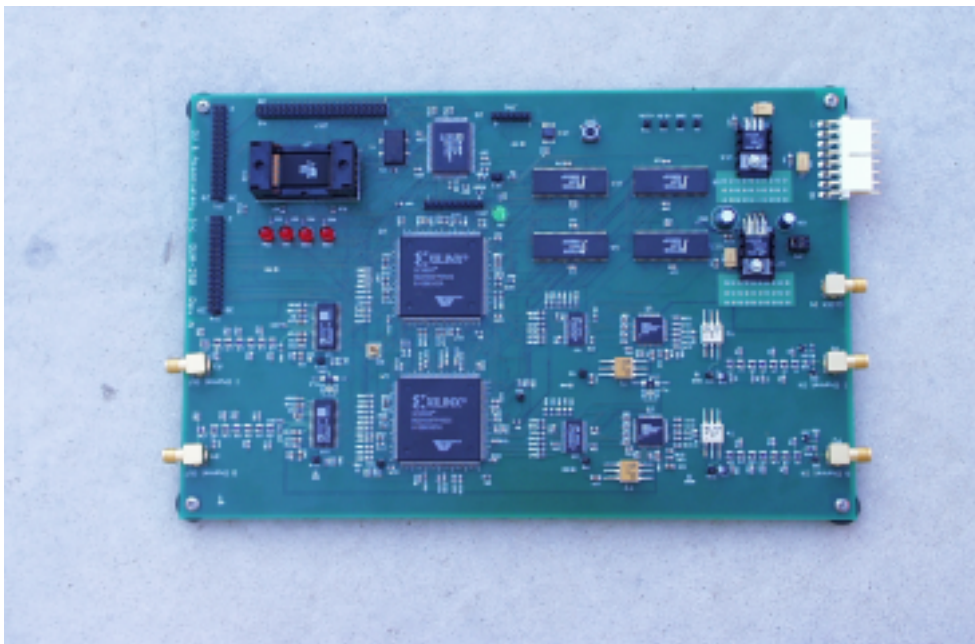

Figure 1:   GVA-250 (Revision A) Virtex DSP Hardware Accelerator

The GVA-250 supports the following Xilinx Virtex FPGAs:

    XCV50-4PQ240C
    XCV100-4PQ240C
    XCV150-4PQ240C
    XCV200-4PQ240C
    XCV300-4PQ240C
    XCV400-4PQ240C
    XCV600-4PQ240C
    XCV800-4PQ240C

Functional Description

The platform's general configuration consists of an I and Q channel which is passed through a 12th order low pass filter. The 12th order low pass filter band limits the input signals to a 30 MHz bandwidth. The signal rejection is -58 dB at 40 MHz. Next, the signals are digitized by a 12 bit A/D. The sample rate (maximum of 65 MHz) of the A/D is programmable using the FPGA. The digitized signals are now ready to be processed by the customer's algorithm that is implemented in hardware by either of the two Xilinx FPGAs. Once the signals have been processed, a 120 MSPS D/A via the Xilinx FPGA convert them back to an analog waveform. The processed data may also be sent to the external data port. The processed analog waveforms are passed through a 12th order smoothing filter which is band limited to 30 MHz. The filtered analog signal is connected to a 50 ohm SMA output for viewing

Each Xilinx FPGA has access to two external 64K x 16 Static RAMs that could be used for temporary data storage. These SRAM may be configured as two independent 64K x 16 bit banks or as a single 128K x 16 bank. Each Xilinx FPGA has up to 114,688 bits of internal Block RAM.

The Xilinx FPGAs may also access unused address space in the configuration EPROM by interfacing to the CPLD via the local bus. Using the 86 bit local bus, the I and Q channel FPGAs could be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processor. Or, the two Xilinx FPGAs could have a 86 bit local bus that allows for the direct transfer of data between the two devices and other external devices. For non-specific clock requirements, an external clock source is available. Each Xilinx FPGA has four Delay Locked Loops (DLL) for system clock synchronization.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

    Xilinx, Inc.
   2100 Logic Drive

    San Jose, CA 95124
    Phone: +1 408-559-7778
    Fax: +1 408-559-7114
    URL: www.xilinx.com

For general Xilinx literature, contact:

    Phone: +1 800-231-3386 (inside the US)
              +1 408-879-5017 (outside the US)
    E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

    Phone: +1 408-879-5381
    E-mail: alliancecore@xilinx.com
    URL: www.xilinx.com/products/logicore/alliance/
    tblpart.htm
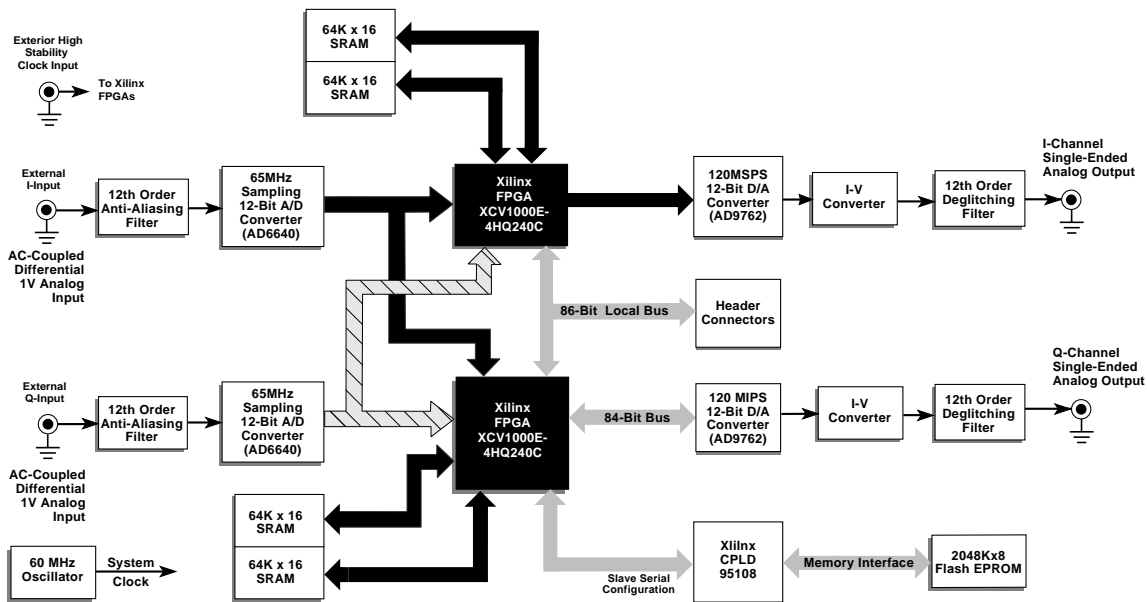
Figure 2: GVA-250 Revision A Virtex-E FPGA Block Diagram