Reed-Solomon Encoder

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Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Programmable solution for high data rate Reed-Solomon encoding
- ISS can configure to support a range of standards involving Reed-Solomon encoding, e.g. European Telecommunication Standard 300 421 and 300 429.
- Architecture can be customized using the following parameters:
  - Symbol size
  - Number of parity symbols
  - Field polynomial
  - Generator polynomial
- Single encoder implementation supports any valid data block length
- Systematic code structure where each code word can be partitioned into original data block and appended parity symbols
- Encoder can process continuous or burst data
- Supports high speed (>570 Mbps) applications
- Symbol-wide inputs and outputs, clocked by a single symbol-rate clock
- Simple interface allows easy integration into larger system

Applications

- Digital video and audio broadcast
- Digital satellite broadcast
- Data storage and retrieval systems (e.g. hard disks, CD-ROM etc)

AllianceCORE™ Facts

Core Specifics	
Supported Family	4000XL, Spartan, Virtex
Device Tested	See Table 1
CLBs	
Clock IOBs	
Performance	
Xilinx Tools	
Special Features	
Provided with Core	
Documentation	Core Documentation
Design File Formats	XNF, EDIF[1] netlist, VHDL RTL Source available extra
Constraints File	.ucf
Verification	Test Vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	Bit-accurate C model is available
Simulation Tool Used	
Synopsys VSS	
Support	
Support provided by ISS.	

Note:
1. Virtex design file format is EDIF.

General Description

The Reed-Solomon encoder is a Xilinx FPGA-based core for systems where data error detection/correction is required. The core implements the full functionality of a general Reed-Solomon encoder and all necessary interface circuitry using a single Xilinx FPGA.

The source code version of the core is extremely flexible due to its parameterized design, and can be rapidly configured for a wide variety of applications. Table 1 shows density and performance metrics for specific implementation examples. ISS will customize and provide a Xilinx-specific implementation of the core tailored to the needs of your application, (see Ordering Information).

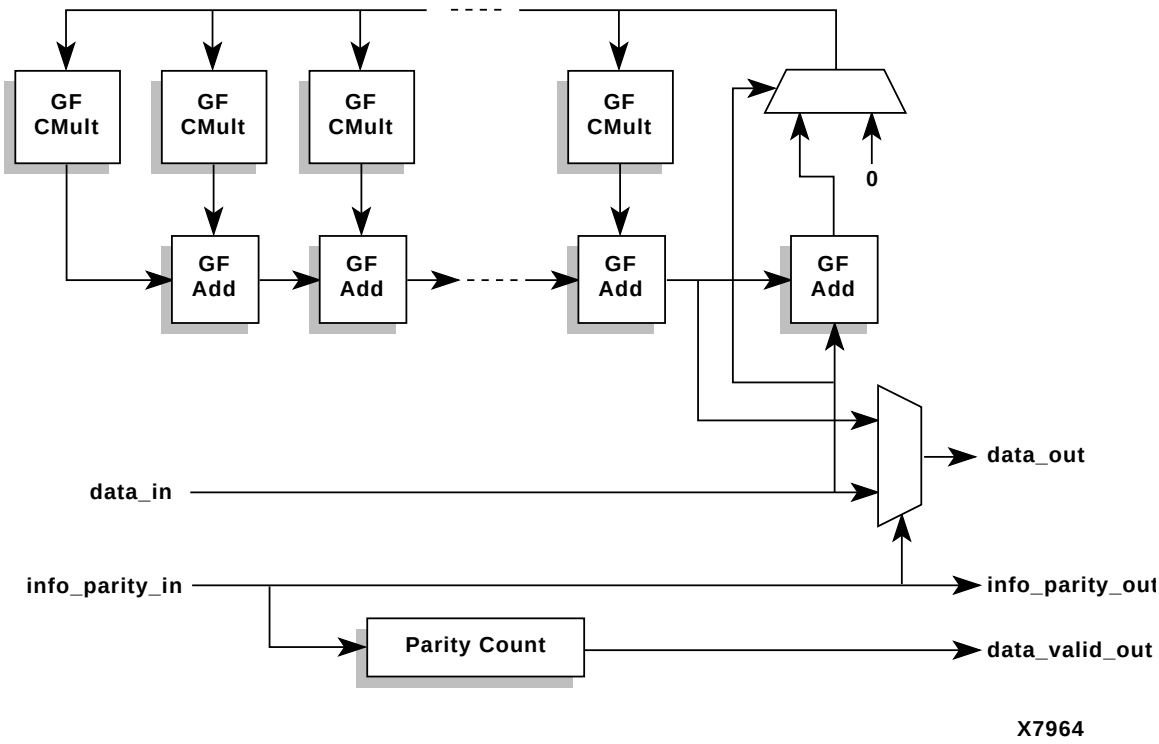

Figure 1: Reed Solomon Encoder Block Diagram

Table 1: Example Encoder Implementations

	Example #1	Example #2	Example #3
Parity Symbols	16	8	16
Bits/Symbol	8	4	8
Device Tested	V50-4	S10-3	4005XL-1
CLBs	82[2]	106	105
Clock IOBs	1	1	1
IOBs[1]	18	12	19
Performance	82 MHz	49.3 MHz	72.2 MHz
Xilinx Tools	M1.5	M1.3	M1.3
Special Features	None	RPM	RPM

Notes:
1. Assuming all I/O are routed off-chip
2. Utilization numbers for Virtex are in CLB slices

Functional Description

The Reed-Solomon encoder core is partitioned into modules as shown in Figure 1 and described below.

GF CMult

This block performs the multiplication of two symbol values over a Galois Field that is defined by the choice of the number of bits per symbol. For example, choosing 8 bits per symbol, the block performs multiplication over GF(2^8). One of the multiplier inputs is a constant, corresponding to a coefficient value from the generator polynomial, which is also customizable by the user. Multiplication is carried out using a bit-parallel, polynomial basis architecture. One GF CMult block is required for each parity symbol to be generated.

GF Add

The GF Add block performs the addition of two symbol values over the appropriate Galois Field.

Parity Count

The parity count block counts the number of parity symbols produced by the encoder for each block of data. The number of valid parity symbols is twice the maximum number of errors that are to be corrected. Any additional symbols produced by the encoder are caused by spurious symbol values that may exist between successive data blocks when burst data is being processed. These spurious symbols are marked in the output data stream by changing the value of the “data_valid_out” signal from high to low.

Pinout

The pinout of the Reed-Solomon Encoder has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram of Figure 1 and in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
DATA_IN [x:0]	Input	Input data symbols
INFO_PARITY_IN	Input	Marks valid input information symbols
CLK	Input	Symbol Clock
RESET	Input	System Reset, active high
DATA_OUT [x:0]	Output	Output data symbols
INFO_PARITY_OUT	Output	Marks valid output information symbols
DATA_VALID_OUT	Output	Marks valid output information and parity symbols.

Verification Methods

The core has been fully tested across a wide range of parameter settings, using input sequences compatible with many international digital video, audio and satellite standards.

Recommended Design Experience

Familiarity with system standards relevant to the particular application is assumed. A basic understanding of Reed-Solomon encoding is useful, but not essential.

Available Support Products

A C model of the Reed-Solomon encoder is available to assist in functional verification and system integration.

ISS also supplies a complete line of peripheral cores that can be integrated with the Reed Solomon Encoder and Decoder cores for a complete forward error correction system using Xilinx FPGAs. For more information, contact ISS directly regarding:

- Block and convolution interleavers and deinterleavers
- Scramblers and descramblers
- Sync detection and insertion
- Convolution encoders
- Viterbi decoders

Ordering Information

The Reed Solomon Encoder is available for purchase directly from ISS. The implementation will vary depending upon your application. To determine what is required for your system, fill out and fax the attached Implementation Request Form to ISS at +44 1232 669664.

Related Information

European Telecommunications Standards Institute

For information on European digital broadcasting systems standards contact:

European Telecommunications Standards Institute
06921 Sophia Antipolis Cedex
France
Phone : +33 92 94 42 00
Fax : +33 93 65 47 16

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Reed-Solomon Implementation Request Form

To: Integrated Silicon Systems, Inc.
FAX: +44 1232 669664
E-mail: info@iss-dsp.com

From: _____

Company: _____

Name: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

ISS configures and ships Xilinx netlist versions of the Reed Solomon cores customized to your specification. Please fill out and fax this form so ISS can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

Implementation Issues

1. Indicate your exact requirement:
   _____ Reed-Solomon encoder
   _____ Reed-Solomon decoder
   _____ Interleaver
   _____ Deinterleaver

2. Maximum symbol rate: _____

3. Number of bits per symbol: _____

4. Indicate clock availability:
   __ ____ Bit clock
   _____ Symbol Clock
   _____ Both

5. Code generator polynomial (e.g. $(x+a^1)(x+a^2)...$)

6. Field generator polynomial (e.g. $x^8+x^4+x^3+x^2+1$)

7. Number of errors: _____

8. Codeword length/format (e.g. 204, 188):

9. Erasure support required:
   Yes _____ No _____

10. Indicate error statistics reporting requirement(s):
    _____ Signal to show position of corrected errors
    _____ Signal to show position of uncorrected blocks
    _____ Other (please specify)

11. Indicate required control signals:
    _____ low to high transition at start of codeword,high to low transition at end of codeword
    _____ low to high transitional start of codeword, high to low transition at start of parity symbols
    _____ delayed control signals available at output
    _____ other (please specify)

12. Please specify any additional requirements:

13. If interleaver and/or deinterleaver functions are required, specify maximum depth of interleaving:

14. If the interleaver and/or deinterleaver are required is the depth of interleaving to be programmable and if so, to what degree?

Business Issues

15. Indicate timescales of requirement:
    a. date for decision _____
    b. date for placing order _____
    c. required delivery date _____

16. Indicate your area of responsibility:
    _____ decision maker
    _____ budget holder
    _____ recommender

17. Has a budget been allocated for the purchase?
    Yes _____ No _____

18. What volume do you expect to ship of the product that will use this core? _____

19. What major factors will influence your decision?
    _____ cost
    _____ customization
    _____ testing
    _____ implementation size

20. Are you considering any other solutions?