DRAM Controller

November 11, 1997 | Product Specification

NMI Electronics Ltd.
Fountain House
Great Cornbow
Halesowen
West Midlands
B63 3BL
United Kingdom
Phone: +44 (0) 121 585 5979
Fax: +44 (0) 121 585 5764
E-mail: ip@nmi.co.uk
URL: www.nmi.co.uk

Features

- Single-chip DRAM controller in a Xilinx XC9500 CPLD
  - Easy to use and modify due to predictable XC9500 timing
- Designed for high speed, high performance applications
- Support for burst mode CPU's
- Utilizes fast page mode or EDO DRAM's
- CAS before RAS refresh
- Supports multiple DRAM types
- Available in source code format for ease of customization
- Compatible with industry standard 72 pin SIMM's

Applications

- Embedded systems in industrial, telecommunications, test or point-of-sale applications
- High performance peripheral equipment, e.g. printers

AllianceCORE™ Facts

Core Specifics	
Device Family	XC9500
Macrocells Used	75[1,4]
IOBs Used	58[1]
System Clock fmax	50+ MHz[2]
Device Features Used	GCLK

Supported Devices/Resources Remaining		
	I/O	Macrocells
XC95216-15 HQ208C[3]	110[1]	141[1]

Provided with Core	
Documentation	Design User Guide Sample files for top level module in VHDL
Design File Formats	VHDL source code
Verification Tool	Viewlogic ViewSim
Schematic Symbols	None
Evaluation Model	Evaluation Board available extra
Reference designs & application notes	Application notes included in Design User Guide
Additional Items	TimingDesigner™ design file

Design Tool Requirements	
Xilinx Core Tools	XACTstep M1.3
Entry/Verification Tool	Viewlogic Workview Office™ 7.4

Support
90 days e-mail and telephone support from NMI Electronics included in the Core price. Support does not cover user core modifications; please refer to "Core Modifications" section. Maintenance contracts available.

Notes:
1. Assumes default configuration, see Functional Description.
2. Depends on device speed selected and other system device speeds. 50MHz operation has been verified with the i486DX4™ and XC95216-15. 40MHz operation has been verified with the same system and XC95216-20.
3. The core has been proven in this device but will work in any XC9500 device with sufficient resources.
4. This number can vary slightly due to device utilization and fitter settings. Typically the number of macrocells varies between 70 and 75 but may be higher in devices with a high utilization and/or speed requirement.

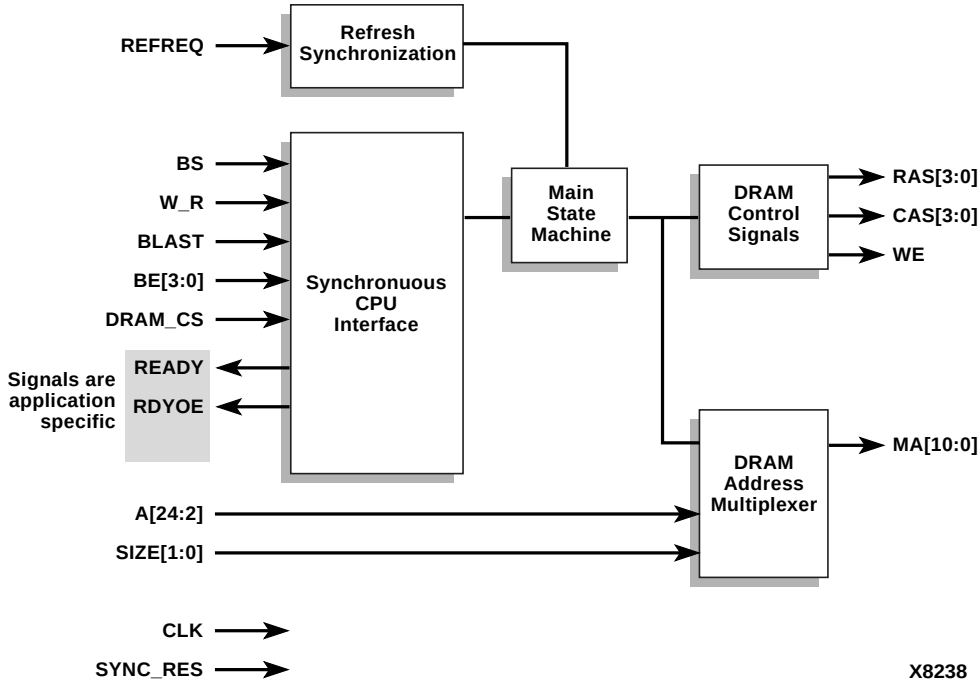

Figure 1: DRAM Controller Block Diagram

General Description

The DRAM Controller is extremely flexible and can be configured to be used with most DRAM types, most microprocessors and many other applications, see Core Modifications.

Functional Description

The DRAM Controller is supplied as a single, VHDL source code module. The functional blocks shown in Figure 1 are for descriptive purposes only.

The default configuration of the DRAM Controller is as follows:

- i486™-like CPU interface, including burst mode
- Two bank, 32 bit wide, 72 pin SIMM compatible DRAM control signals
- Support for 256K, 1M and 4M bit deep DRAM's

Synchronous CPU Interface

In order to achieve maximum performance the DRAM Controller utilizes a fully synchronous interface to its host CPU or control logic. This does not, however, prevent the user from adding extra logic to create an asynchronous interface.

Main State Machine

The DRAM Controller is state machine driven. The state machine, along with the input clock frequency, controls the timing of the DRAM signals.

Refresh Synchronization

Refresh requests are not automatically generated by the DRAM Controller as these can often be generated using other, lower frequency clocks which are available in many typical system designs. Due to this fact, the DRAM Controller fully supports asynchronous refresh request inputs.

DRAM Control Signals

The DRAM control signals RAS, CAS and WE are synchronously generated from the state machine outputs. Burst mode is supported using page mode, refresh utilizes CAS-before-RAS, while writes use “early write” mode.

DRAM Address Multiplexer

The DRAM address multiplexer can be configured to support most DRAM sizes and organizations. The Design User Guide describes this process in detail.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
CLOCK	Input	Primary system clock; rising edge triggered.
SYNC_RES[1]	Input	System reset, synchronous to CLOCK; active High.
BS	Input	Bus cycle start signal; active High. One CLOCK period wide. Identical to inverse of i486™ ADS signal.
W_R[1]	Input	System read or write cycle indicator. Cannot change state during whole bus cycle, or during a complete burst sequence; 0=read 1=write.
BLAST[1]	Input	Burst last indicator. Active High for last bus cycle in a burst sequence.
BE[3:0][1]	Input	Byte enable signals for default, 32 bit configuration. Writes are gated by state of byte enables; however all reads return 32 bit data; active Low.
DRAM_CS[1]	Input	Select signal for DRAM Controller; active High. Must be active while BS is active for DRAM Controller to respond to a bus cycle. Usually driven by an address decode.
A[24:2][1]	Input	System address lines for default, 32 bit configuration; active High.
SIZE[1:0]	Input	DRAM module size selection inputs. These should not be changed during normal system operation. For default configuration these are: 00 - 256 KBit DRAM's 01 - 1 MBit DRAM's 1x - 4 MBit DRAM's
REFREQ	Input	Refresh request input; active High. May be asynchronous to CLOCK, and is rising edge triggered. Typical period is 15.625 microseconds maximum.
RAS[3:0]	Output	DRAM RAS outputs; active Low. To be compatible with standard 72 pin SIMM's, RAS0 and RAS1 are functionally identical and drive half of the first bank of DRAM's each. RAS2 and RAS3 drive half of the second bank of DRAM's each.
CAS[3:0]	Output	DRAM CAS outputs; active Low; Configured for fast page mode operation by default and used in early-write mode, when CAS activation is gated by their respective BE's.
WE	Output	DRAM WE output; active Low. DRAM Controller uses early-write mode, so WE is used as an indicator only.
MA[10:0]	Output	Multiplexed row and column address outputs; active High. Multiplexing scheme determined by state of SIZE inputs.
READY	Output	System Ready output; active High. Default configuration is for i486™ microprocessor. Output is usually system host specific.
RDYOE	Output	System Ready 3-state enable output; active High. Default configuration utilizes a 3-state driver for System Ready. Output is usually system host specific.

Note:

1. These signals must be applied synchronously to CLOCK.

Core Modifications

As supplied, the DRAM Controller is designed for optimum performance in the 40MHz to 50MHz range, using 70ns fast-page-mode DRAM's. The system interface is i486™-like.

Many system designs will require that the core be modified before it can be used, especially with regard to the system interface. For this reason the core is supplied in source code format, and has been written with modification in mind.

The Design User Guide supplied with the core describes in detail how the core can be modified for different system

interfaces, different clock speeds and different DRAM types and speeds.

Please note that NMI support does not cover user core modifications. NMI offers design services, including core modifications, for additional cost.

Pinout

The pin functions of the DRAM Controller core in its default configuration are shown in Table 1. The pinout is not fixed to any specific CPLD I/O, and can generally be modified to suit the user's application.

Signal names are provided in the block diagram shown in Figure 1, and described in Table 1.

Verification Methods

Both functional and timing simulation have been carried out using ViewSim under Viewlogic Workview Office™. Simulation vectors used for verification are provided with the core in the form of ViewSim command files.

The core has been extensively tested on target hardware using an NMI developed evaluation card.

Recommended Design Experience

Users should be familiar with VHDL and Xilinx design flows. Experience with microprocessor or similar system design is recommended. The core can easily be integrated into hierarchical VHDL designs.

Available Support Products

NMI has developed a Xilinx core evaluation card and this will be available, at additional cost, in the near future.

Ordering Information

To make further enquiries or purchase the DRAM Controller Core, please contact NMI directly at the location detailed on the front page. NMI also offers core integration and design services, the latter covering not only CPLD and FPGA design but also complete systems design.

NMI cores are purchased under a Licence Agreement, copies of which are available on request.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm