Synchronous DRAM Controller

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Features

- Single-chip SDRAM controller in a Xilinx Virtex, XC4000XL FPGA, or XC9500 CPLD
  - parameterizable for each architecture
  - XC9500 core is easy to use and modify due to predictable timing
  - Virtex/XC4000XL core allows the SDRAM Controller to be integrated into much larger designs
- Low gate count, high speed, high performance solution
- SDRAM refresh capability

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Design User Guide
Design File Formats	VHDL source RTL[1]
Verification Tool	VHDL Testbench
Instantiation Templates	VHDL
Reference designs & Application notes	None
Additional Items	Hardware demo board available
Simulation Tool Used	
Model Technology ModelSim™ 4.7i.	
Support	
90-day e-mail and telephone support from NMI Electronics included in the core price. Support does not cover user core modifications; please refer to “Core Modifications” section. Maintenance contracts available.	

Notes:
1. Synplify v5.1.4 used for synthesis.

Table 1: Example Core Implementation Data

	Example # 1	Example # 2	Example # 3	Example # 4	Example # 5	Example # 6
System Interface	**i486™**	**i486™**	**i486™**	**i486™**	**i486™**	**i486™**
# of SDRAM types[1]	1	2	1	1	1	1
# of SDRAM banks	1	2	1	1	1	1
Persistent page mode?	yes	yes	no	yes	yes	yes
Supported Family	Virtex	Virtex	Virtex	4000XL	4000XLA	9500XL
Device Tested[2]	V50-6	V50-6	V50-6	4013XL-2	4013XLA-07	95144XL-5
CLBs	40[3]	54[3]	32[3]	44	41	81[4]
Clock IOBs	1	1	1	1	1	1
IOBs	58	61	58	58	58	58
Performance	123MHz	108MHz	137MHz	72MHz	105MHz	125MHz
Xilinx Tools	M1.5i	M1.5i	M1.5i	M1.5i	M1.5i	M1.5i
Special Features	DLL	DLL	DLL	None	None	None

Notes:
1. Number of SDRAM types is set by number of allowable combinations of SIZE[1:0] and COL[1:0], with a maximum of 16 combinations.However, use of the full 16 combinations results in a very large and slow core which is not typical of actual designs.
2. The core has been proven in these devices but will work in similar devices with sufficient resources.
3. Utilization numbers for Virtex are in CLB Slices.
4. Utilization numbers for 9500XL are in Macrocells.

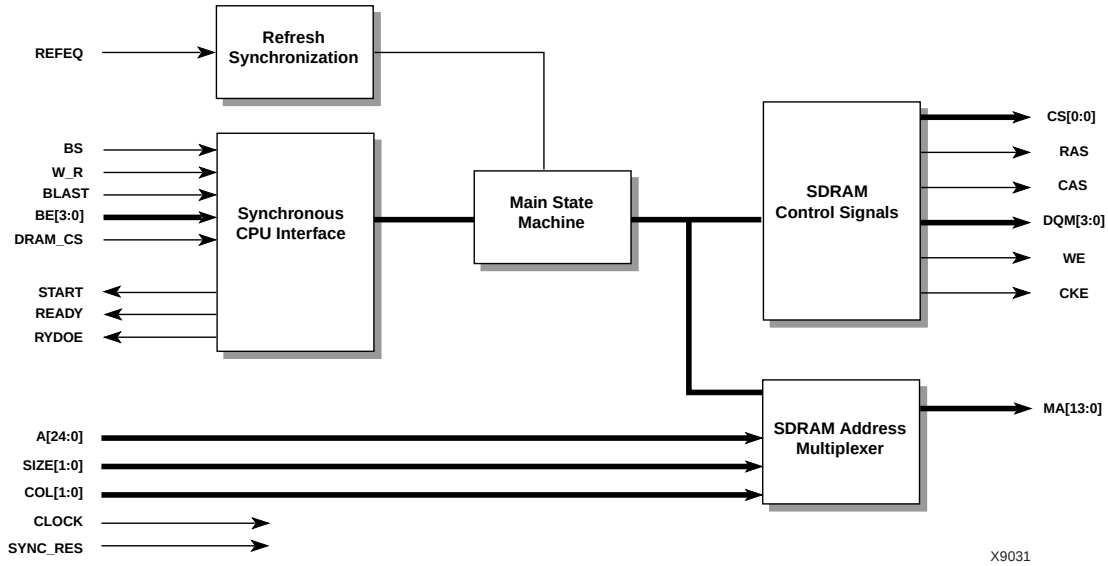

Figure 1: SDRAM Controller Block Diagram

Features (cont.)

- Source code format for easy customizing; complete VHDL development flow
- Highly parameterizable, VHDL “Generic” based design allows easy customizing of:
  - SDRAM physical device type
  - SDRAM array width
  - Number of SDRAM banks
  - SDRAM interface timing
  - SDRAM initialization
  - Burst modes (all types supported)
  - Optional auto-precharge mode
  - System interface

Applications

- Embedded systems in industrial, telecommunications, test or point-of-sale applications
- High performance peripheral equipment, e.g. printers

General Description

The SDRAM Controller is extremely flexible due to its VHDL Generics and can be configured to be used with most SDRAM types, most microprocessors and many other applications (see Core Modifications).

Functional Description

The SDRAM Controller is supplied as a VHDL source code. Additional Xilinx constraints file is provided with FPGA cores. The functional blocks shown in Figure 1 are for descriptive purposes only. The default configuration of the SDRAM Controller is as follows:

- i486™-like CPU interface, including 4-word burst mode
- Single bank, 32-bit wide SDRAM array
- Support for typical 4M, 16M and 64M bit SDRAMs in x4, x8 or x16 organizations
- Supports persistent page mode operation for optimal CPU performance
- Typical CAS Latency=3 SDRAM timing

The SDRAM Controller can be configured to provide automatic SDRAM initialization, or this task can be delegated to external logic, allowing some level of dynamic reconfiguration of the SDRAMs.

Synchronous CPU Interface

In order to achieve maximum performance the SDRAM Controller utilizes a fully synchronous interface to its host CPU or control logic. This does not, however, prevent the user from adding extra logic to create an asynchronous interface.

Main State Machine

The SDRAM Controller is state machine driven. The state machine, along with the input clock frequency, controls the timing of the SDRAM signals.

Refresh Synchronization

Refresh requests are not automatically generated by the SDRAM Controller as these can often be generated using other, lower frequency clocks which are available in many

typical system designs. Due to this fact, the SDRAM Controller fully supports asynchronous refresh request inputs.

SDRAM Control Signals

The SDRAM control signals CS, RAS, CAS, DQM, WE and CKE are synchronously generated from the state machine outputs. All SDRAM burst modes are supported and refresh utilizes CBR (auto) refresh.

SDRAM Address Multiplexer

The SDRAM address multiplexer can be configured to support many SDRAM sizes and organizations. Typical 4, 16 and 64 Mbit devices are supported in x4, x8 and x16 organizations. Multiple SDRAM sizes and/or organizations can be supported by a single build of the core, although this does impact speed and area. The Design User Guide describes the configuration process in detail.

Core Modifications

As supplied, the SDRAM Controller is configured for SDRAMs running in a typical CAS Latency of 3 mode. The system interface is i486™-like.

Many system designs will require that the core be modified before it can be used, especially with regard to the system interface. For this reason the core is supplied in source code format, and has been written with modification in mind. Also the SDRAM interface has a very complete set of VHDL “Generics” (see above), allowing easy modification of the core without altering any source code. NMI can configure the FPGA version of the core to customer specification and provide necessary files to guarantee design performance.

The Design User Guide supplied with the core also describes in detail how the core can be modified for different system interfaces, different clock speeds and different SDRAM types and speeds.

Please note that NMI support does not cover user core modifications. NMI offers design services, including core modifications, for additional cost.

Pinout

The pin functions of the SDRAM Controller core in its default configuration are shown in Table 2. The pinout is not fixed to any specific FPGA or CPLD I/O, and in many cases can be modified to suit the user’s application.

Signal names are provided in the block diagram shown in Figure 1, and described in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
System Interface Signals		
BS	Input	Bus cycle start signal; active High. One CLOCK period wide. Identical to inverse of i486™ ADS signal.
W_R	Input	System read or write cycle indicator. Cannot change state during whole bus cycle, or during a complete burst sequence; 0=read 1=write.
BLAST	Input	Burst last indicator. Active High for last bus cycle in a burst sequence.
BE[3:0]	Input	Byte enable signals for default, 32 bit configuration. Writes are gated by state of byte enables; however all reads return 32 bit data; active Low. Actual bus width set via VHDL Generic.
DRAM_CS	Input	Select signal for SDRAM Controller; active High. Must be active while BS is active for DRAM Controller to respond to a bus cycle. Usually driven by an address decode.
START	Output	Indicates that a System access to SDRAM is pending.
READY	Output	System Ready output; active High. Default configuration is for i486™ microprocessor. Output is usually system host specific.
A[24:2]	Input	System address lines for default, 32 bit configuration; active High.
RDYOE	Output	System Ready 3-state enable output; active High. Default configuration utilizes a 3-state driver for System Ready. Output is usually system host specific.
CLOCK	Input	Primary system clock: rising edge triggered.

Table 2: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
SDRAM Interface Signals		
CS[0:0]	Output	SDRAM CS (chip select) output; active Low. VHDL Generic allows 1 or 2 chip selects to be supported.
RAS	Output	SDRAM RAS output; active Low.
CAS	Output	SDRAM CAS output; active low.
DQM[3:0]	Output	SDRAM DQM outputs; active Low. VHDL Generic allows any byte width to be supported.
WE	Output	SDRAM WE output; active low.
CKE	Output	SDRAM CKE output; active high.
MA[13:0]	Output	Multiplexed row and column address outputs; active High. Multiplexing scheme determined by state of SIZE and COL inputs.
Other Signals		
REFREQ	Input	Refresh request input; active High. May be asynchronous to CLOCK, and is rising edge triggered. Typical period is 15.625 microseconds maximum.
SIZE[1:0]	Input	SDRAM module size selection input. This should not be changed during normal system operation. For default configuration this is: 00 - 4 MBit SDRAMs 01 -16 MBit SDRAMs 1x - 64 MBit SDRAMs
COL[1:0]	Input	SDRAM column address lines selection input. For default configuration this is: 00 - 8 CAS address lines 01- 9 CAS address lines 1x - 10 CAS address lines
SYNC_RES	Input	System reset, synchronous to CLOCK; active High.

Verification Methods

Functional simulation has been carried out using Model Technology's ModelSim™4.7i. The VHDL testbench used for verification is provided with the core.

The core has been extensively tested on target hardware using an NMI developed evaluation card that is available for purchase separately. NMI has also used the core to fulfill some of its own design services contracts.

Recommended Design Experience

Users should be familiar with VHDL and Xilinx design flows. Experience with microprocessor or similar systems design is recommended. The core can easily be integrated into hierarchical VHDL designs.

Available Support Products

NMI has developed a Xilinx core evaluation card for XC4000XL and XC9500 architectures and this is available at additional cost.

Ordering Information

To make further enquiries or purchase the SDRAM Controller Core, please contact NMI directly at the location detailed on the front page. NMI also offers core integration and design services, the latter covering not only CPLD and FPGA design but also complete systems design.

NMI cores are purchased under a Licence Agreement, copies of which are available on request. NMI retains the right to make changes to these specifications at any time, without notice. All trademarks, registered trademarks, or servicemarks are the property of their respective owners.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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