MT1F T1 Framer

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Features

- DS1/ISDN - Primary Rate Interface Framing transceiver
- Frames to D4, ESF, and SLC-96 formats
- Control through Microprocessor interface
- Extracts and inserts robbed - bit signaling
- Programmable output clocks
- FDL support logic circuitry
- Fully independent Transmitter and Receiver block
- Pay load and Local loopback capability
- Loop up/down code generation and detection capability
- Extensive status indication

Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces
- High speed computer to computer data links
- Digital cross-connect interface

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000EX	
CLBs Used	1296	
IOBs Used	37[1]	
System Clock fmax	1.544 MHz	
Device Features Used	N/A	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4036EX-3 HQ240	156[1]	0
Provided with Core		
Documentation	Core Specification Document	
Design File Format	.ncd and .nga files Verilog Source RTL avail extra	
Constraint Files	.ucf	
Verification Tool	Test Vectors	
Schematic Symbols	None	
Evaluation Model	None	
Reference Designs and Application Notes	None	
Additional Items	None	
Provided with Core		
Xilinx Core Tools	Alliance 1.3	
Verification Tool	Verilog XL Simulator	
Support		
Support provided by Virtual IP Group.		

Note:

1. Assuming all core signals are routed off-chip.

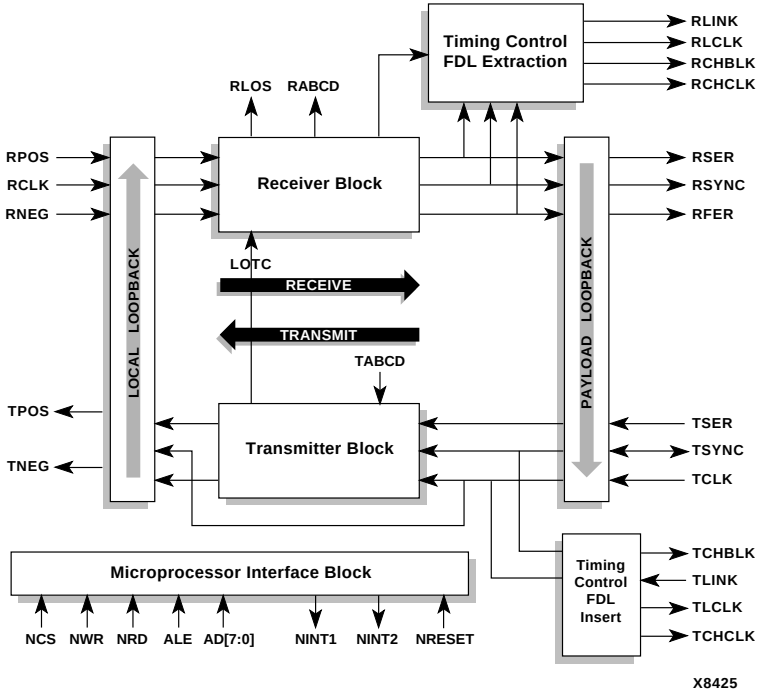

Figure 1: MT1F T1 Framer Block Diagram

General Description

The MT1F is a comprehensive, software-driven T1 framer core. It can be interfaced to a standard microcontroller or microprocessor data bus. The MT1F is very flexible and can be configured into numerous orientations via software. The core provides a set of 60 8-bit internal registers which the user can access to configure the core and obtain information from the T1 link. The core fully meets all of the latest T1 specifications including ANSI T1.403-1989, AT&T TR 62411 (12-90), and CCITT G.704 and G.706.

The MT1F core is compatible with the existing D4 framing standard described in AT&T PUB 43801 and the new extended superframe format (ESF) as described in AT&T C.B# 142. The salient differences between the D4 framing and ESF framing formats are the number of frames per superframe and use of the F-bit position (refer to tables 4&5). In the D4 framing 12 frames make up a superframe; in ESF, 24. A frame consists of 24 channels (times slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

Functional Description

Functionally the MT1F T1 Framer core can be divided into three main sections: the Receiver block, the Transmitter block, and the Microprocessor interface block. The block diagram is shown in Figure1.

Receiver Block

On the receive side, the device will clock in the serial T1 stream via the RPOS and RNEG signal lines. The synchronizer will locate the frame and multiframe patterns and establish their respective positions. This information is used by the rest of the receive side circuitry.

The MT1F is an “off-line” framer, which means that all of the T1 serial stream that goes into the device will come out unchanged. Once the T1 data has been framed, the robbed-bit signaling data and FDL can be extracted. The receiver block provides the logic for B8ZS decoder, Bipolar violation detection and counting, synchronizer, alarm detection, loop code detection, CRC generation and detection, error counting for CRC and Frame error, signaling extraction and channel marking.

Transmitter Block

The transmit side clocks in the unframed T1 stream at TSER and adds in the framing pattern, the robbed-bit signaling, and the FDL. The Transmit block includes logic required for functions like F bit insertion, idle code insertion, clear channel, signaling insertion, loop code generation, Bit 7 stuffing, CRC generation, FDL insertion, Yellow alarm generation and insertion, AIS generation and B8ZS encoder.

Microprocessor Interface Block

The Microprocessor interface contains a multiplexed address and data bus input and output data bus with output enable which can be connected to either a Microcontroller or Microprocessor.

Core Modifications

Virtual IP Group can perform modifications on the Xilinx netlist version of this core for additional cost. This includes adding or removing blocks, or creating a different controller interface.

An Elastic Store function (in Verilog source format only) is available for additional cost. Contact Virtual IP Group for more information.

Pinout

Signal names for the core are shown in Figure 1 and described in Table 1.

Verification Methods

The FPGA core was tested through simulation.

Recommended Design Experience

Users should be familiar with T1 and related standards as well as Xilinx design flows.

Ordering Information

This product is available directly from Virtual IP Group, Inc. Please contact them for further information or pricing.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Transmitter Interface Signals		
TPOS	Output	Transmit Bipolar Positive Data: Updated on rising edge of TCLK. NRZ data is output when TCR1.7 = 1.
TNEG	Output	Transmit Bipolar Negative Data: Updated on rising edge of TCLK. Zero is output when TCR1.7 = 1.
TSER	Input	Transmit Serial Data: Transmit NRZ serial data, sampled on falling edge of TCLK.
TSYNC	I/O	Transmit Sync: A pulse on TSYNC will set either frame or multiframe boundaries. Can be programmed to output either a frame or multiframe pulse; can also be set to output double-wide pulses at signaling frames.
TCLK	Input	Transmit Clock: 1.544 MHz Primary clock.
TCHBLK	Output	Transmit Channel Block: output; can be forced high or low during any of 24 T1 channels.
TLINK	Input	Transmit Link Data: If enabled, TLINK will be sampled during F-bit time on falling edge of TCLK for data insertion into either FDL stream (ESF) or Fs bit position (D4).
TLCLK	Output	Transmit Link Clock: 4 KHz demand clock for TLINK input.
TCHCLK	Output	Transmit Channel Clock: 192 KHz clock pulses high during LSB of each channel.
TABCD	Input	Transmit ABCD signaling: When enabled, data on this line is sampled on negedge of TCLK and inserted into the transmitted NRZ stream at signaling frames.
Receiver Interface Signals		
RPOS	Input	Receive Bipolar Positive Data Input: Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Signal	Signal Direction	Description
RCLK	Input	Receive Clock: 1.544 MHz primary clock.
RNEG	Input	Receive Bipolar Negative Data Input: Sampled on falling edge of RCLK.
RLINK	Output	Receive Link Data: Updated with FDL data (ESF) or Fs bits (D4) one RCLK before start of frame.
RLCLK	Output	Receive Link Clock: 4 KHz demand clock for RLINK.
RCHBLK	Output	Receive Channel Block: programmable, can be forced high or low during any of 24 T1 channels.
RCHCLK	Output	Receive Channel Clock: 192 KHz clock, pulses high during LSB of each channel.
RSER	Output	Received NRZ Serial Data; updated on rising edges of RCLK.
RSYNC	Output	Receive Sync: An extracted pulse, (one RCLK wide) identifies either frame or multiframe boundaries. Can also be set to output double-wide pulses on signaling frames.
RFER	Output	Receive Frame Error: High during F-bit time when Ft or Fs errors occur in D4 mode or when FPS or CRC errors occur in ESF mode. Low during resync.
RABCD	Output	Receive ABCD signaling: Outputs received signaling data.
LOTC/RLDS	Output	Receive Loss of Sync/Loss of Transmit Clock: dual function. If CCR1.6=0, signal will toggle high when synchronizer is searching for T1 frame and multiframe. If CCR1.6=1, signal will toggle high when TCLK has not been toggled for 5µs.
Microprocessor Interface Signals		
NCS	Input	Chip Select: must be low to access internal registers (for read or write).
NWR	Input	Microprocessor Write signal.
NRD	Input	Microprocessor Read signal.
ALE	Input	Address Latch Enable: serves to demultiplex bus.
AD(7:0)	In/Out	Multiplexed Address/Data Bus: 8-bit multiplexed address/data input bus. For addressing internal registers, only AD(5:0) are decoded.
NINT1	Output	Receive Alarm Interrupt 1: Flags host controller during alarm conditions defined in Status Register 1.
NINT2	Output	Receive Alarm Interrupt 2: Flags host controller during conditions defined in Status Register 2.
NRESET	Input	Reset input: Active low reset. Minimum pulse width should be one clock period (either TCLK/RCLK) duration.