Parallel to Serial Converter

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Features

- Support 2 to 32 bit word lengths
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro accepts a parallel N-bit value and loads it into a shift register when the **L** (LOAD) and **CE** (CLOCK ENABLE) signals are active. With **L** inactive and **CE** active, data in the shift register is shifted by one bit position on each rising edge of the Clock. Both the parallel contents of the shift register and the serial data are presented at the module's outputs **PO[n:0]** and **SDO.** The Truth Table for this function is shown in Table 1.

Table 1: Truth Table

LOAD	CE	C	PO[n:0] (SDO = PO[0])
X	0	_/-	No Change
0	1	_/-	PO[n] <= SDI, PO[n-1:0] <= PO[n:1]
1	1	_/-	PI[n:0]

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 2.

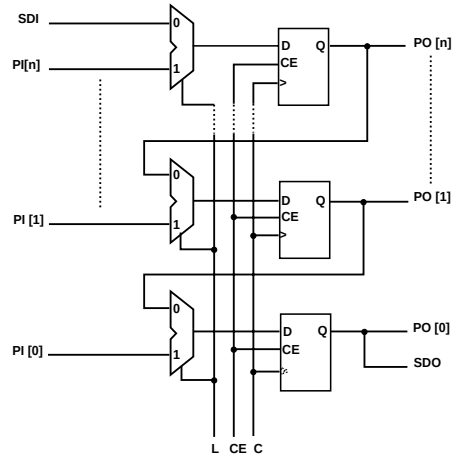

Figure 1: Functional Block Diagram

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
PI[n:0]	Input	PARALLEL DATA INPUT – value is captured when the L (LOAD) and CE (CLOCK ENABLE) signals are asserted.
SDI	Input	SERIAL DATA IN – Serial Data Input. Value on this pin is loaded into the MSB of the shift register when L is inactive and CE is active
L	Input	LOAD – when this signal is asserted, the data on PI[n: 0] is loaded in to the shift register. The CE signal must be asserted for the load operation to occur.
CE	Input	CLOCK ENABLE – active high signal used to enable the shift register for both shift and load modes of operation.

Signal	Signal Direction	Description
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
SDO	Output	SERIAL DATA OUTPUT – Connected internally to PO[0].
PO[n:0]	Output	PARALLEL DATA OUTPUT – Parallel output of the shifted register. This output can be used for serial to parallel conversion when used in association with SDI.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Port Width**: Select a bit width from the pull-down menu. The valid range is 2-32.
- **Create RPM**: When checked, a columnar Relational Placed Macro is created.

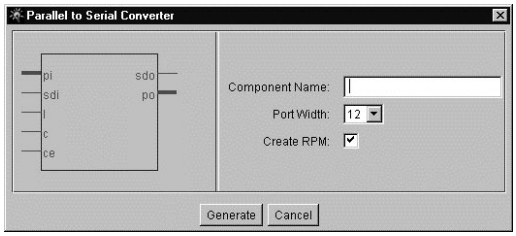

Figure 2: Parameterization Window

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	1
3	2
4	2
5	3
6	3
7	4
8	4
9	5
10	5
11	6
12	6
13	7
14	7
15	8
16	8
17	9
18	9
19	10
20	10
21	11
22	11
23	12
24	12
25	13
26	13
27	14
28	14
29	15
30	15
31	16
32	16

Parameter FIle Information

Parameter Name	Type	Notes
Component_name	String	
Port_Width	Integer	2 - 32
Create_RPM	Boolean	True/False