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Application Note: CoolRunner™ CPLDs

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XAPP302 (v1.2) October 9, 2000

Metastability Characteristics for CoolRunner CPLDs

Introduction

When using a latch or flip-flop in normal circumstances (i.e., when the devices setup and hold times are not being violated) the outputs will respond to a latch enable or clock pulse within some specified time. These are the propagation delays found in the data sheets. If, however, the set-up and hold times are violated so that the data input is not a clear one or zero, there is a finite chance that the flip-flop will not immediately latch a high or low but get caught half way in between. This is the metastable state and it is manifested in a bistable device by the outputs glitching, going into an undefined state somewhere between a high and low, oscillating, or by the output transition being delayed for an indeterminable time.

Once the flip-flop has entered the metastable state, the probability that it will still be metastable some time later has been shown to be an exponentially decreasing function. Because of this property, a designer can simply wait for some added time after the specified propagation delay before sampling the flip-flop output so that he can be assured that the likelihood of metastable failure is remote enough to be tolerable. On the other hand, one consequence of this is that there is some probability (albeit vanishingly small) that the device will remain in a metastable state forever. The designer needs to know the characteristics of metastability so that he can determine how long he must wait to achieve his design goals.

The following information on the Xilinx CPLDs is provided to fill this basic need to know how the device operates in situations where metastability may be a problem. It is important in evaluating the reliability of your system that you obtain and evaluate this information from any programmable logic supplier you may be using. Also note that metastable characteristics are different at operating corners of supply voltage and temperature ranges—be wary of data that is presented only at room temperature and nominal V_{CC}.

Metastable Characteristics

Table 1 presents the metastability data for Xilinx 3V CoolRunner CPLDs, manufactured on our 0.5 µm EECMOS process. Table 2 presents this data for Xilinx 5V CoolRunner CPLDs. As shown, Xilinx provides complete data on the XCR3032s metastable characteristics. While the XCR3032 does not employ Xilinx patented metastable immune flip-flops, its metastable characteristics are still quite favorable relative to competitive devices.

Table 1: **Metastability Data for Xilinx 3V CPLDs**

	0°C		25°C		70°C	
	τ	T_0	τ	T_0	τ	T_0
3.0V	95.0 ps	1.43E+13	101.0 ps	4.83E+12	113.0 ps	5.91E+11
3.3V	86.7 ps	1.53E+13	90.3 ps	1.98E+13	103.0 ps	1.41E+12
3.6V	80.7 ps	2.50E+17	84.10 ps	1.17E+15	93.70 ps	7.75E+12

Table 2: **Metastability Data for Xilinx 5V CPLDs**

	0°C		25°C		70°C	
	τ	T_0	τ	T_0	τ	T_0
4.75V	68.4 ps	2.87E+14	71.3 ps	3.11E+14	76.6 ps	2.45E+14
5.0V	66.6 ps	8.47E+14	69.9 ps	3.75E+14	74.8 ps	4.90E+14
5.25V	66.2 ps	9.07E+14	68.5 ps	1.08E+15	73.7 ps	8.38E+14

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Design Example

Suppose a designer wants to use the XCR3032 for synchronizing asynchronous data that is arriving at 10 MHz (as measured by a frequency counter), in a 3.3V system that has a clock frequency of 50 MHz, at an ambient temperature of 25°C. The next device in the system samples the output of the XCR3032 8 ns after the clock edge to ensure that any metastable conditions that occur have time to resolve to the correct state. The MTBF for this situation can be calculated by using equation below:

$$MTFB = \frac{e^{(t'/\tau)}}{(T_0 F_C F_1)}$$

In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' > T_{CO}). T_0 and τ are device parameters provided by the semiconductor manufacturer. T_0 and τ are derived from tests and can be most nearly defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_0 is a function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a normalization constant which is a very strong function of the normal propagation delay of the device.

In this situation the F 1 will be twice the data frequency, or 20 MHz, because input events consist of both low and high transitions. Thus, in this case F_C is 50 MHz, F_1 is 20 MHz, τ is 90.3 ps, t' is 8 ns, and T_0 is 1.98 x 10^{13} seconds. Using the above formula the actual MTBF for this situation is 1.51 x 10^{10} seconds or 478.6 years for theXCR3032.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/14/00	1.1	Converted to Xilinx format.
10/09/00	1.2	Added Discontinuation Notice.