XAPP331 (v1.1) October 9, 2000

Reclaiming XPLA1 ISP with V_{PP} Bulk Erase

Summary

This document provides a description of how to perform a V_{PP} mode bulk erase of an XPLA1 CPLD. This procedure requires that a supervoltage be applied to the V_{PP} pin, and that several other pins be manipulated in order to successfully erase the device.

Introduction

In-System Programmable devices span the density range from small PLDs (such as 22v10s) to FPGAs with hundreds of I/O pins. JTAG configurable programmable logic requires the use of four dedicated pins (sometimes five, if TRESET is used) to implement the control and data shifting that is required to correctly program any device. While this "pin cost" is not much of a burden for devices with hundreds of pins, lower density devices may find themselves I/O restricted and the use of four I/O pins for JTAG functions may seem like a large imposition on pin availability.

XPLA1 ISP devices have the ability to assign I/O signals to these JTAG pins, however doing so will remove the access to the TAP controller which shuts down the port and renders the ISP functions useless. Any XPLA1 ISP devices that have had a bulk erase performed (which is how all XPLA1 CPLDs are shipped) will have the JTAG port enabled as a default state. User created JEDEC files for these devices leave the ISP pins enabled; a user has to consciously force the TAP controller off in order to reclaim the JTAG pins for I/O use. A JEDEC file that assigns signals to the JTAG pins may be downloaded via ISP one time; the loading of this file onto a CPLD will turn off the ISP port as described above. Once the ISP function is turned off, it will fail to be recognized in an ISP chain or as a single ISP device.

Reclamation of the ISP functionality has typically been accomplished by removal of the device form the PCB and then performing a manufacturing bulk erase (V_{PP} Mode) on a stand-alone programming device. However, there is a technique which may be used to perform this same bulk erase while the device is still on the PCB which involves the application of a supervoltage, and the manipulation of some of the I/O pins. This technique and the identification of the necessary control pins will be covered in detail in this document.

Overview

The bulk erase procedure may only be performed on a device that has been properly powered up; the device must have had a monotonic V_{CC} ramp and the power supply must be of low enough impedance to provide the necessary inrush current for startup (typically 50 to 100 mA for 20 µs). Once the device is powered up, a manufacturing bulk erase requires that a supervoltage be applied to the V_{PP} pin, and that the control pins P/E, VFY, SDIN, STR, and SCLK be manipulated with attention to required timing. It is critical that designers pay close attention to the manipulation of the control pins and especially the V_{PP} pin. Signal contention or

Special Note:

Because of the unusual technique described in this application note, signal contention and/or overvoltage damage is possible; users must proceed with caution and at their own risk. Xilinx does not state nor imply any warranty associated with this technique, and is not responsible for damage that may result due to the implementation of this technique.

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overvoltage damage is likely; users must proceed with caution. Refer to Figure 1 for a waveform diagram, and Table 1 for timing information.

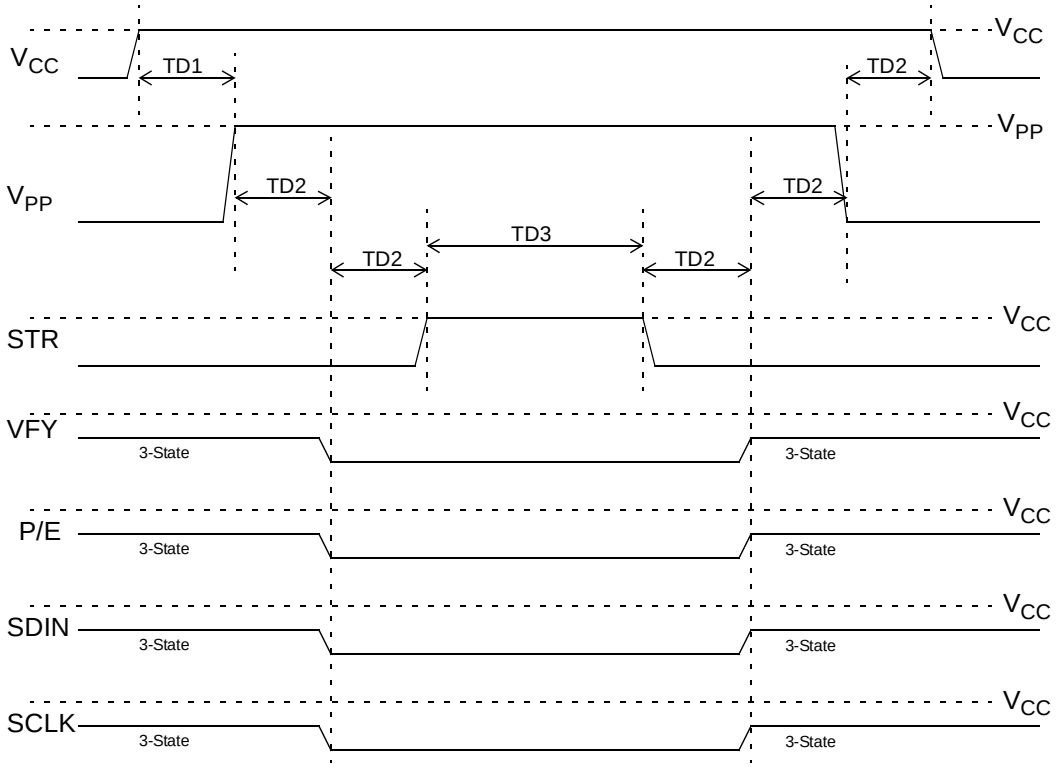

Figure 1: **Bulk Erase Waveform Diagram**

Table 1: **Bulk Erase Timing Delays**

Symbol	Delay (min)
TD1	100 µs
TD2	2 µs
TD3	100 ms

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Pin Identification

Pin identification is not specified for manufacturing control pins in the standard datasheet; the pin assignments for the pins required for Bulk Erase are called out in Table 2. It is important to note that pin compatibility (manufacturing control pins) may not exist for devices of different densities who share a common package.

Table 2: **Pin Assignments for V_{PP} Bulk Erase**

Part	Package	Pin Number
XCR5032C/N XCR3032C/N XCR3032A/D	44 PLCC	V_{PP} = 1 STR = 2 VFY = 4 P/E = 5 SDIN = 7 SCLK = 32
XCR5032C/N XCR3032C/N XCR3032A/D	44 TQFP	V_{PP} = 39 STR = 40 VFY = 42 P/E = 43 SDIN = 1 SCLK = 26
XCR5064C/N XCR3064A/D	44 PLCC	V_{PP} = 1 STR = 2 VFY = 4 P/E = 6 SDIN = 7 SCLK = 32
XCR5064C/N XCR3064A/D	44 TQFP	V_{PP} = 39 STR = 40 VFY = 42 P/E = 44 SDIN = 1 SCLK = 26
XCR5064C/N XCR3064A/D	100 TQFP	V_{PP} = 89 STR = 90 VFY = 92 P/E = 98 SDIN = 4 SCLK = 62
XCR3064A/D	56 LFGBA	V_{PP} = C6 STR = C5 VFY = C4 P/E = A2 SDIN = C1 SCLK = F10

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Table 2: **Pin Assignments for V_{PP} Bulk Erase**

Part	Package	Pin Number
XCR5128 XCR3128	84 PLCC	V_{PP} = 1 STR = 2 VFY = 4 P/E = 10 SDIN = 14 SCLK = 62
XCR5128 XCR3128	100 PQFP	V_{PP} = 91 STR = 92 VFY = 94 P/E = 1 SDIN = 6 SCLK = 64
5128 3128 5128C/N 3128A/D	100 TQFP	V_{PP} = 89 STR = 90 VFY = 92 P/E = 99 SDIN = 4 SCLK = 62
5128 3128 5128C/N 3128A/S	128 LQFP	V_{PP} = 116 STR = 117 VFY = 119 P/E = 127 SDIN = 8 SCLK = 82
5128 3128	160 PQFP	V_{PP} = 141 STR = 142 VFY = 144 P/E = 152 SDIN = 9 SCLK = 99

V_{PP} Information

The V_{PP} voltage that must be applied to perform this procedure is nominally 12V DC with a deviation of ±0.25V. The power supply for V_{PP} must be capable of sourcing this potential at a load of 25 mA. For all XPLA1 devices, the nominal V_{PP} value is 12V. When V_{PP} is applied to the device, internal circuitry senses this condition and places all of the I/O signals into 3-state.

Conclusion

Xilinx does not recommend this procedure be implemented as part of standard design technique, because of the risks associated with placing a supervoltage onto a system board. If an end user has inadvertently or purposely turned off the ISP port on an XPLA1 device, it is possible to perform an erase of the part (and thereby reclaiming the TAP port) without removing the part from the PCB for erasure on a stand alone programmer.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
2/18/00	1.0	Initial release.
10/09/00	1.1	Added Discontinuation Notice.

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