NEW Virtex-EM FPGAs Over 1-Mbits of RAM

Xilinx extends the Virtex family; new FPGAs use copper interconnect technology for optimized performance.

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Many high-performance applications in networking and video processing require large amounts of on-chip RAM. To meet this demand, Xilinx recently announced the Virtex™-E Extended Memory (Virtex-EM) FPGA family that is the first in the industry to provide over one megabit of True Dual PortTM Block RAM and is also the first to offer copper interconnect for optimized performance.

Features

The Virtex-EM family builds on the highly successful Virtex architecture and includes the following:

- Two devices: XCV405E and XCV812E.
- Over 1-Mbit of True Dual-Port RAM (XCV812E).
- Leading edge 0.18 micron, 6-layer metal silicon process.
- New copper interconnect used for top two layers:
  - Top layer for uniform on-chip power distribution
  - Second layer for clock signals - minimizes clock skew
- Support for 20 I/O standards, including LVDS, Bus LVDS, and LVPECL differential signaling standards.
- Over 311 Mbps single-ended I/O performance.
- 622 Mbps differential I/O performance.
- Complete hierarchy of memory resources.
- Eight DLLs for over 311 MHz clock management.
- Direct interface to high-performance external memory.

Applications

Virtex FPGAs are used in communications, networking, and video image processing applications, where the inherent flexibility of the architecture allows you to efficiently implement powerful data path and digital signal processing (DSP) operations.

Xilinx primarily developed the Virtex-EM family to address the application requirements of our large networking customers. The unique combination of block RAM and logic, along with copper interconnect, allows increased data bandwidth and greater integration; this gives networking companies a very efficient and reliable platform for their 160 Gbps switch fabrics.

The Virtex-EM family also addresses high-end video processing, which uses DSP engines to improve image quality and implement video compression and decompression algorithms. By using the large block RAM capacity, both the line buffer memory and either a video processing engine or a DSP function can be accommodated on the same Virtex-EM device, which greatly enhances the overall system bandwidth.

Availability and Pricing

Samples of the XCV812E are available now, and the XCV405E will be sampled in June. Both devices are expected to be in full production in third quarter this year. The XCV812E and the XCV405E devices are priced at $235 and $101, respectively for 50,000 units in Q4 2000.

For more information on the Virtex-EM FPGA family see: http://www.xilinx.com/products/ virtex/ss_virem.htm.