The World's Highest-performance Programmable DSP Solution. A New Paradigm in High Performance Digital Signal Processing...

by Rufino Olay
Sr. DSP Product Marketing Engineer, Xilinx
rufino.olay@xilinx.com

Xilinx DSP consists of the Virtex and Spartan series FPGAs, a wide range of DSP algorithms, and a comprehensive set of software tools and prototyping boards. This is a complete DSP solution giving you the high performance and system integration of ASICs and ASSPs plus the reconfigurability and quick turnaround of standard processors. This ultimate combination provides a comprehensive and robust platform to help you create the highest performing reprogrammable signal processing applications imaginable.

We've created a complete design flow that guides you through the conceptual architectural design, verification, and implementation. Design techniques such as parallel processing and distributed arithmetic, coupled with industry-leading hardware platforms, increases sampling rates by an order of magnitude over that of traditional approaches; there is no faster DSP solution, anywhere. Table 1 shows a sample listing of algorithm benchmarks.

Algorithm	Benchmark	Unit of Measure
16-bit	160,000,000,000	MAC/s
256 Tap FIR	160	MSPS
1024 pt FFT	41	usec
Reed Solomon Decoder	87	MHz
JPEG Codec	21	MHz
ADPCM	16	MHz

Table 1 - Performance Matrix

Fast, Flexible, and Easy

With Xilinx DSP you can easily create customized architectures that give you the best speed and area utilization for your particular needs.

Parallel Operations

Xilinx DSP helps you create the most robust DSP applications by exploiting the parallelism that is inherent in DSP mathematical models. Using the vast logic resources that are present in the Virtex FPGAs, you can create fully parallel structures that give you the utmost in computational power.

Customizable Data Structures

Unlike fixed-width processors or ASICs, Xilinx FPGAs give you the freedom to create custom word lengths for your particular situations, including different parameters within the same design. For example some channels in your system might require more bits of precision than others; you can easily change the algorithm and the Xilinx DSP software will easily accommodate the new data configuration.

Multiple Data Paths and Channels

Individual arithmetic logic can be linked to separate data paths or mutually coupled to run parallel operations during individual cycles. This approach is ideal for applications consisting of multiple subtasks that need little or no interdependency.

Logical Operations

You can easily implement a variety of bit- and byte-wide operations such as barrel shifting, comparison, rotation, and accumulation by instantiating any of our numerous cores or by writing your own HDL code to customize a particular process.

The MathWorks Simulink Integration

Xilinx and The MathWorks (the leader in DSP algorithm tools) have created a strategic alliance that allows you to build high performance DSP systems in Xilinx FPGAs using the system design and verification tools with which you are already familiar. The result is the Xilinx System Generator™ tool-set which bridges the gap between your conceptual architectural design and the actual translation and implementation of your FPGA-based DSP system.

With the Xilinx System Generator you can easily experiment with various DSP functions and quickly see the algorithmic tradeoffs between performance and silicon area.

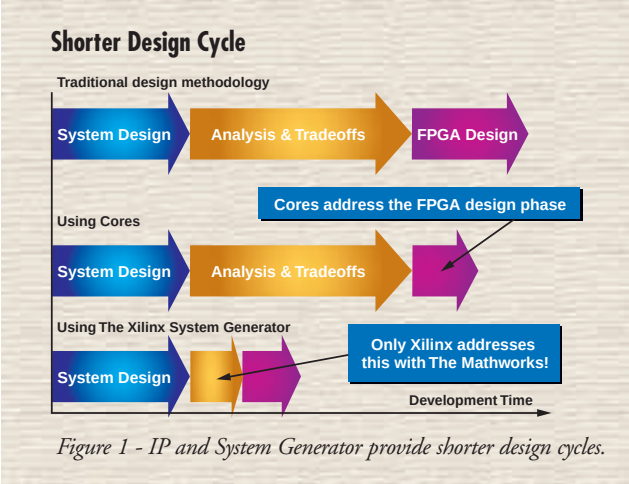

Figure 1 - IP and System Generator provide shorter design cycles.

Then you can easily compare the cost and speed with off-the-shelf DSP devices.

Key Features include:

- Seamless integration; no manual redesign is required.
- No risk of error introduction.
- Only one source code to maintain.
- Floating-point and fixed-point system simulation.
- Automatically generates HDL description for Xilinx FPGAs.

Comprehensive IP Offering

Our extensive selection of IP, including filters, correlators, transforms, FFTs, FECs, integrators, DDS, and math functions, gives you the power to build large, complex designs quickly and effortlessly. Plus, our IP is optimized and parameterized for implementation in our Virtex and Spartan FPGAs so you get the most efficient and fastest implementation.

The intuitive GUI in our CORE Generator guides you through the various options to help you customize the IP for your specific design requirements. The features include:

- Scalable IP to fit your particular application.
- Millions of possible permutations.
- Minimal learning curve.

New FIR Filter Generator

Xilinx recently announced the FIR Filter Generator, a new tool for creating fully optimized and parameterized algorithms for FPGA-based complex single-rate, half-band, Hilbert transform, and interpolated filter designs. Design techniques such as distributed arithmetic are employed to optimize filter structures for high-end DSP applications such as wireless and xDSL modems, medical imaging, and radar signal processing. The operational performance of the FIR filters, in the Virtex family, exceeds 160 billion multiply accumulates (MACs) per second.

The FIR Filter Generator allows you to choose from millions of parameter combinations to match your unique DSP design requirements, from fast, fully parallel systems to cost-effective designs optimized for lower sampling rates, as shown in Figure 2. The available parameters include:

- From 2 to 1024 taps.
- From 1 to 32 bit input data and coefficient precision.
- Signed or unsigned input data.
- Fully serial, parallel, or a combination of serial/parallel filter implementations with the ability for multi-clocking of output data.
- Time multiplexing of data for multiple channel structures.

Smart-IP Technology

By employing the Xilinx Smart-IP Technology, the CORE Generator maintains constant performance over the entire range of FPGA densities; Smart IP gives you predictable timing and optimal an implementation for area and speed. This predictability, unique to Xilinx, is essential for incorporating entire systems on an FPGA.

In-House Expertise

We've gathered together a highly knowledgeable team of DSP experts to create the best possible DSP tools and to provide you the best possible design expertise. In addition, Xilinx DSP FAEs have extensive design experience which gives them particular insight and knowledge to the challenges and intricacies of high performance DSP applications.

Third-Party Programs

To help you further reduce your development time, Xilinx has partnered with various DSP development companies to provide a wide range of services, from algorithm development to full turnkey operation, giving you:

- A large and growing selection of system IP from our AllianceCORE partners.
- Access to the leading DSP experts in various application areas.
- Design services and expertise from the Xilinx XPERTS partners.
- A wide range of in-house and third-party design expertise and application experience.

In addition, numerous third-party vendors such as GV & Associates, Nallatech, and Lyr Signal Processing also offer prototyping hardware.

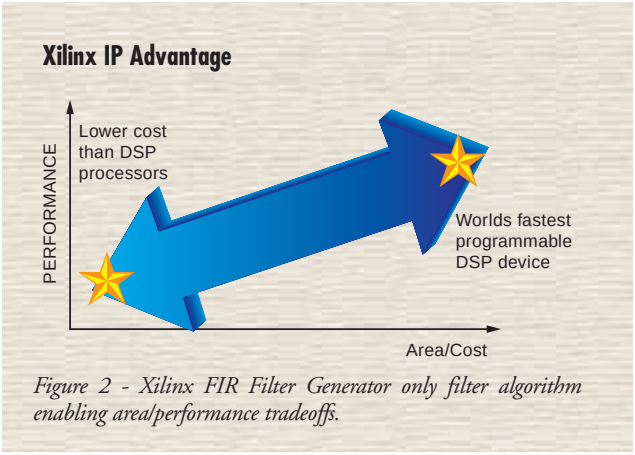

Figure 2 - Xilinx FIR Filter Generator only filter algorithm enabling area/performance tradeoffs.

Conclusion

With the Xilinx DSP solution, you get faster DSP designs that are customized for your exact needs. Plus, there are no NRE charges or limitations to your creativity. There simply is no better way to create DSP designs.

For more information see www.xilinx.com/dsp