LavaCORE - A Configurable Java Processor

Create Java-enabled appliances, mobile devices, secure Internet devices, and embedded network computers that can be dynamically configured for application-specific computing.

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LavaCORE™ is a 32-bit configurable Java™ processor core targeted to the Xilinx Virtex FPGA architecture. The processor executes Java bytecode directly in hardware eliminating the need for software-based interpreters or code translators. LavaCORE is a clean-room implementation of the Java Virtual Machine and is provided as a synthesizable "soft-core" with a suite of tools for parameterized core generation, hardware/software co-design, co-verification, and custom Java application development.

LavaCORE is a revolutionary product that provides unparalleled flexibility for a wide range of prototyping and embedded applications. Direct Java bytecode execution keeps the runtime to a minimum making the processor ideal for embedded applications that require small memory foot-prints and flexible reconfigurable architectures. Both the application and the operating system code can be developed in Java and compiled to native code by standard Java compilers.

LavaCORE is designed to bring embedded Java technology to the reconfigurable marketplace. The customizable core and dynamic reconfiguration take full advantage of the features of programmable hardware.

LavaCORE Features

The processor core features a 32-bit architecture with 32-bit address and data paths. Our reference design is implemented in a Virtex XCV300 BG352-4 FPGA. Figure 1 shows a block diagram of the architecture.

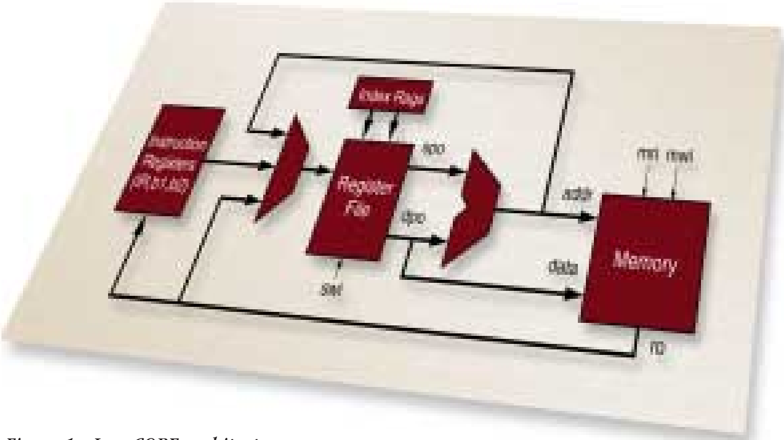

Figure 1 - LavaCORE architecture.

A 16x32-bit dual-ported RAM implements the register-file. The instruction register is composed of three 8-bit registers denoting the instruction, byte one, and byte two of the instruction stream. A 32-bit ALU computes arithmetic and logical operations. Additional signals include clock, reset, signal interrupt, memory interface, and a set of observability pins for the state and flags.

Some of the features are highlighted below:

- 32-bit direct execution Java processor.
- Executes Java Virtual Machine bytecode in hardware.
- Stand-alone (system on a chip) or core configuration.
- Built-in hardware encryption module.
- Fully synthesizable FPGA core.
- Parameterized Core Generator automatically synthesizes VHDL, Verilog, or EDIF gate-level netlists.
- Software support includes Parameterized Core Generator, LavaOS Runtime Environment, Co-Simulation/Verification Tools, and Hardware Debugger.

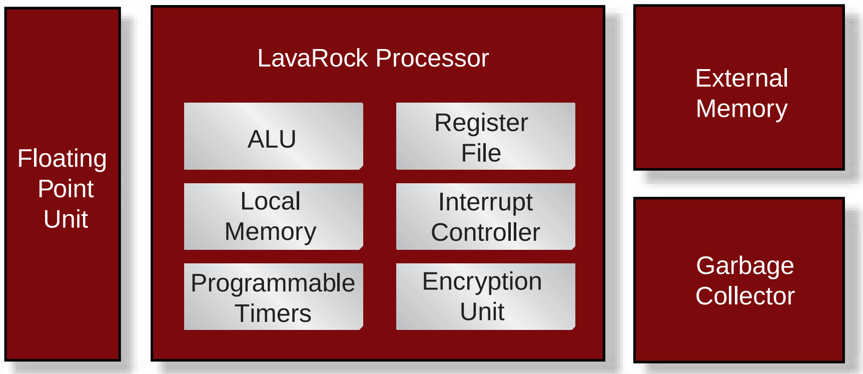

Figure 2 - LavaCORE system architecture.

Parameterized Core Generator

The LavaCORE Parameterized Core Generator operates via an intuitive graphical interface and includes user selectable parameters for a wide range of configurable options. Every implementation of LavaCORE can be application specific, leading to optimal solutions in terms of power, speed, and area.

Typically, specialized embedded applications use only a subset of the full JVM instruction set. By analyzing the application, you can determine which Java bytecode instructions can be omitted or moved from hardware to software, improving various cost criteria.

Additional options allow you to include functional components of the synthesized architecture such as the built-in encryption engine, programmable timers, and interrupt controllers. For larger systems, floating point and external memory interfaces are defined (Figure 2).

Once parameterized options are selected, the LavaCore Generator automatically synthesizes a gate-level implementation in either VHDL, Verilog, or EDIF netlist formats. Along with this softcore, an HDL testbench and a customized runtime called LavaOS™ are generated.

The synthesized core can then be directly input to Xilinx Foundation Series or Alliance Series software for place and route. The HDL testbench is used both to test the hardcore and softcore. Figure 1 depicts the dataflow architecture of a LavaCore instance.

Linker/Application Builder

Standard Java-class files, generated from third party commercial Java development environments, are statically resolved to build executables. In addition, the linker builds the boot tables, class initialization codes, and assigns the interrupt and trap handlers.

The executable image incorporates the runtime environment. It is designed for embedded applications and is small enough to be implemented in the internal block RAM. In a standalone configuration, the LavaCORE system architecture can incorporate the entire runtime environment and a Java application within the Virtex block RAM.

Application Debugging Tools

The LavaCore application debugging tool set consists of a core simulator and a hardware interface (Figure 3). The simulator has a built-in debugger that features single stepping, memory and register file monitors, and conditional break points. The simulator and the debugger share a graphical user interface to display and debug the LavaCore execution both at instruction and micro steps.

The LavaCore simulation environment consists of three separate components that validate all three aspects of the LavaCore:

- The instruction tester.
- The application simulator.
- The hardware testbench for the synthesized core.

The hardware interface provides an implementation debugging bridge for the synthesized hardware. The same debugging environment and user interface are used for the testing of the target hardware.

Conclusion

The LavaCORE Configurable Java Processor core enables the deployment of Java technology for a new generation of embedded reconfigurable systems. Native execution of Java bytecode provides reliable hardware execution, denser code, and minimum runtime environment. The LavaCORE parameterized core generator allows you to configure the capabilities of the processor core and synthesize an optimal LavaCORE for your application.

LavaCORE provides a fast design solution for embedded Java processors targeted to programmable hardware. With our configurable Java processor core and co-design/verification environment this unique IP product will reduce design time leading to faster time to market.

For more information about Derivation Systems, or the LavaCORE products, see www.derivation.com

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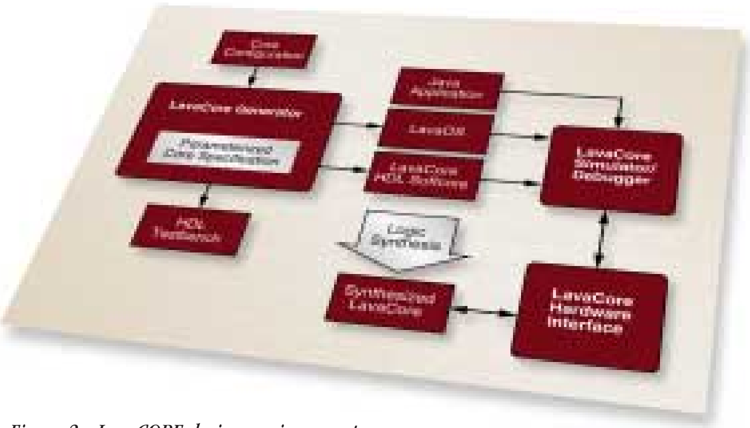

Figure 3 - LavaCORE design environment.