Choices, Choices, and Opinions

How to choose the best Xilinx programmable logic technology for your application.

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Xilinx offers a wide variety of programmable logic devices, using different architectures and technologies. Here is a high-level overview of the different families and some suggestions for the prospective user.

5V or 3.3V / 2.5V?

The standard logic supply for 30 years has been 5 volts, but modern processes with smaller geometries demand lower voltages, such as 3.3V, 2.5V, 1.8V, and even lower in the future. While Xilinx strives to make inputs tolerant to voltages higher than Vcc, we discourage you from starting any new project with 5V devices.

Xilinx will continue offering 5V devices for years to come, but these devices will not benefit from the traditional performance enhancing and cost-reducing redesigns, and process enhancements. To benefit from the latest technology, do not use 5V devices for new designs unless there is a special reason.

CPLDs or FPGAs?

CPLDs with their PAL-derived, easy-to-understand, AND-OR structure offer a single-chip solution with fast pin-to-pin delays, even for wide input functions. And, once programmed, the design can be locked and thus made secure. Most CPLD architectures are very similar, so it is important to evaluate the subtle nuances.

In-system-programmability (ISP) is a must for today's designs, and the ability to maintain pin-outs during design modifications ("pin-locking") is crucial. The limited complexity (<300 flip-flops) means that most CPLDs are used for "glue logic" functions. For most CPLDs, the relatively high static (idle) power consumption prohibits their use in battery-operated equipment. Xilinx CoolRunner devices are the notable exception, offering the lowest static power consumption (<50 microamps) of any programmable device.

FPGAs offer much higher complexity, up to 70,000 flip-flops, and their idle power consumption is reasonably low. Because the configuration bitstream must be reloaded every time power is re-applied, design security is an issue, but the advantages and opportunities of dynamic reconfiguration, even in the end-user system, are an important advantage. FPGAs offer more logic flexibility than CPLDs, and more sophisticated system-level features (clock management, on-chip RAM, programmable I/O levels).

Recommendations

Use CPLDs, such as the XC9500XL family, for small designs where "instant-on", fast and wide decoding, in-system programmability, and design security are important. Use CoolRunner CPLDs when idle-power consumption is important, as in battery-operated equipment.

Use FPGAs for larger and more complex designs.

FPGA Families

Xilinx has a wide range of FPGAs to choose from. Here's an overview of our complete product line, from the beginning.

XC2000 and XC6200

The Xilinx XC2000 family was introduced in 1985, and has outlived its useful life. The XC6200 family embodied an innovative architecture that was popular in academic research, but found no commercial use. These families are no longer available.

XC3000, XC3100, and XC5200

These families are not recommended for new designs, because several newer families offer better functionality and performance at a lower price. The XC3000L is still the FPGA family with the lowest static (idle) power consumption of <100 microamps, and it offers an on-chip crystal-oscillator driver, not available in any other FPGA family. These families stay in production, but are not recommended for new designs.

XC4000 - E, EX, XL, XLA, and EV

Today, this is the industry's most popular series of FPGA families. The XC4000E is a superset of the XC4000 family, with higher speed, more routing, and edge-triggered synchronous write into the LUT-based RAM. The XC4000EX extends the XC4000E family to 3000 flip-flops, and adds a generous amount of routing resources. The XC4000,

XC4000E, and XC4000EX are 5V families, and as such are not generally recommended for new designs, because newer families offer better performance and lower cost.

The 3.3V XC4000XLA is an upgrade of the very popular 3.3V XC4000XL family, and the 2.5V XC4000XV extends the family to 18,000 flip-flop capacity. The XC4000XLA devices should be used where the more advanced features of the Virtex series (BlockRAM, clock management, and versatile I/O) are not needed. Use Virtex-E instead of XC4000XV for new designs.

Spartan

Spartan devices are functionally a subset of the XC4000E family, offering up to 2000 flip-flops at a significantly lower price. They are mainly used in cost-sensitive, high-volume (consumer) applications. Spartan FPGAs achieve lower manufacturing cost in several ways:

- The die are smaller.
- The manufacturing flow is streamlined.
- Speed, temperature, and package options are more limited.
- Configuration modes are bit-serial only.
- The pricing structure favors high-volume sales.

Spartan is a 5V family, and as such is not generally recommended for new designs.

Spartan-XL and XC4000XLA

The Spartan-XL and XC4000XLA families offer similar features and performance, where Spartan-XL covers the range of 360 to 2000 flip-flops, while XC4000XLA offers 1,500 to 7,000 flip-flop capacity. These 3.3V families should be used where the more advanced features of the Virtex series and Spartan-II are not needed (such as BlockRAM, clock management, and versatile I/O).

Virtex, Virtex-E, and Virtex-EM

The Virtex family is the biggest design project in Xilinx history and, judging by the number of early design-wins, is also the most successful. The Virtex architecture is rooted in XC4000 concepts (4-input look-up tables, usable as synchronous RAM), but the design started with a clean slate:

- The interconnect structure is generous, and is optimized for short and predictable delays.
- DLL-based fully digital clock-management eliminates on-chip and on-board clock delays.
- The device pins are compatible with many board-level I/O standards.
- Up to several hundred dual-ported BlockRAMs of 4Kb each.

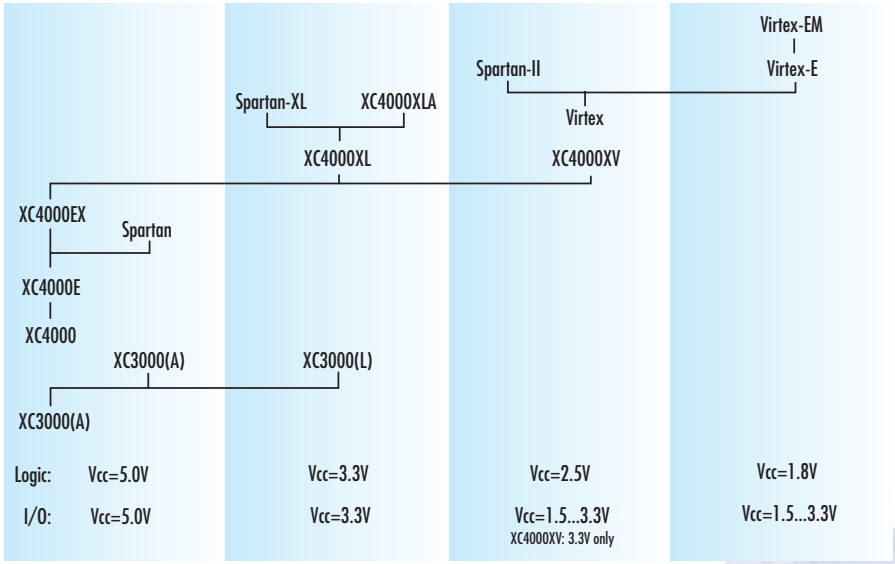

Figure 1 - Xilinx FPGA Genealogy

The 2.5V Virtex family covers the range from 1,800 to more than 27,000 flip-flops. The 2.5V Virtex pins are 5V tolerant, and the devices can implement 5V PCI.

The 1.8V Virtex-E family is an enhanced superset of the original Virtex family with two or three times the amount of BlockRAM, as well as support for differential I/O standards such as LVDS, BusLVDS, and LVPECL. At the high end, Virtex-E offers 73,000 flip-flops (>3 million system gates). The enhanced 0.18 micron process provides higher performance, but requires 1.8V for the core. The I/O uses up to 3.3 V, and is not 5V tolerant.

The 1.8V Virtex-EM family includes two devices that are electrically and architecturally identical with Virtex-E, but have significantly more BlockRAM (over 1 million bits in the XCV812E). Virtex-EM is also the first FPGA family using copper interconnect technology for lower interconnect resistance, higher speed, and better resistance to metal-migration problems.

The Virtex-E and -EM families are highly recommended for new designs, where they offer not only high speed and high capacity, but also valuable system-level features such as clock management, a versatile I/O structure, and substantial amounts of dual-ported BlockRAM. Virtex-EM is ideal for memory-intensive applications.

Spartan-II

Spartan-II extends the advanced features of the Virtex family, with 400 to 4,700 flip-flops. Spartan-II uses streamlined manufacturing methods and limited speed, temperature, and package options to address the cost-sensitive high-volume (consumer) market.

Conclusion

Xilinx offers many different programmable logic families to meet the needs of a wide range of applications. Make sure you are using the right technology today, so your designs will continue to be competitive tomorrow.