QPRO QML-Certified FPGAs and PROMs

The Xilinx QPRO family of Radiation Hardened FPGAs and PROMs are finding homes in many new satellite and space applications. Both the XQR4000XL and XQVR Virtex products are being designed into space systems that will utilize reconfigurable technology. Numerous communications and GPS satellites, space probe, and shuttle missions are included on the growing list of programs that will be flying these devices.

The Virtex QPRO family of High Reliability products is experiencing a high degree of success in the defense market. As designers find it more and more difficult to find components suitable for the harsh environments seen by defense systems, they are discovering that they can incorporate the functions of obsolete parts into Virtex QPRO products. This has the added long term advantage of significantly reducing the costs of future re-qualifications, because their systems can retain consistent form, fit, and function through the use of Virtex QPRO FPGAs. This cannot be achieved with costly and inflexible ASICs or custom logic.

Please visit http://www.xilinx.com/products/hirel_qml.htm for all the latest information about these products, including some new applications notes.

FPGA Product Selection Matrix

		DENSITY							FEATURES						
DEVICES	KEY FEATURES	Logic Cells	Maximum Logic Gates	Typical System Gate Range	Max. RAM Bits	CLB Matrix	CLBs	Flip-Flops	Max. I/O	Output Drive (mA)	PCI Compliant	1.8 Volt	2.5 Volt	3 Volt	5 Volt
XQR/XQ4013XL	XC4000 Series: Density Leadership/ High Performance/ SelectRAM Memory	1368	13K	10K-30K	18K	24x24	576	1536	192	12/24	Y	–	–	X	*
XQR/XQ4036XL		3078	36K	22K-65K	42K	36x36	1296	3168	288	12/24	Y	–	–	X	*
XQR/XQ4062XL		5472	62K	40K-130K	74K	48x48	2304	5376	384	12/24	Y	–	–	X	*
XQ4085XL		7448	85K	55K-180K	100K	56x56	3136	7168	448	12/24	Y	–	–	X	*
XQV100	Virtex Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O 4 DLLs	2700	32K	72K-109K	78K	20x30	600	2400	180	2/24	Y	–	X	I/O	*
**XQVR/XQV300		6912	83K	176K-323K	160K	32x48	1536	6144	316	2/24	Y	–	X	I/O	*
**XQVR/XQV600		15552	187K	365K-661K	312K	48x72	3456	13824	512	2/24	Y	–	X	I/O	*
**XQVR/XQV1000		27648	332K	622K-1,124K	512K	64x96	6144	24576	512	2/24	Y	–	X	I/O	*

* I/Os are tolerant
** XQR and XQVR devices are Radiation Hardened
X = Core and I/O voltage
I/Os = I/O voltage supported

(1) All devices specified from -55°C to +125°C
(2) Selected XQ4000E/EX devices also available

QPRO QML-certified PROMs

		Package			
Device	Density	DD8	SO20	CC44	PC44
XC1736D	36Kb	X			
XC1765D	64Kb	X			
XC17128D	128Kb	X			
XC17256D	256Kb	X			
XQR/XQ 1701L*	1Mb		X	X	
XQR/XQ 1704L*	4Mb			X	X**

* XQR devices are Radiation Hardened.
** XQ devices only.

Xilinx development systems give you the speed you need. With version 3.1i solutions, Xilinx place and route times are as fast as 2 minutes for our 200,000 gate, XC2S200 Spartan(r)-II device, and 30 minutes for our 1 million gate, system-level XCV1000E Virtex(tm)-E device. That makes Xilinx development systems the fastest in the industry.

And with the push of a button, our timing-driven tools are creating designs that support I/O speeds in excess of 800 Mbps, and internal clock frequencies in excess of 300 MHz.

These development solutions combine powerful technology with a flexible, easy to use graphical interface to help you achieve the best possible designs within your project schedule, regardless of your experience level.

Lead Product Feature Comparison

	Alliance Series		Foundation Series				ISE Series		
	ALI-STD	ALI-ELI	FND-EXP	FND-ELI	FND-BAS	FND-BSX	ISE-ELI	ISE-EXP	ISE-BSX
Design Entry									
Schematic Entry			√	√	√	√	√	√	√
HDL Entry			√	√	√	√	√	√	√
ABEL Entry			√	√	√	√	√	√	√
HDL Editor			√	√	√	√	√	√	√
State Diagram Editor			√	√	√	√	VSS*	VSS*	VSS*
Environment									
Operating System	PC/UNIX	PC/UNIX	PC	PC	PC	PC	PC	PC	PC
Simulation									
Gate Level Timing Simulation			√	√	√	√			
HDL Simulation	MTI**	MTI**	MTI**	MTI**	MTI**	MTI**	MTI**	MTI**	MTI**
HDL Test Bench Generator							VSS*	VSS*	VSS*
Synthesis									
Xilinx Synthesis Technology (XST)							√	√	√
FPGA Express			√	√	√	√	√	√	√
Incremental Synthesis			√	√	√	√	√	√	√
System Features	**ALI-STD**	**ALI-ELI**	**FND-EXP**	**FND-ELI**	**FND-BAS**	**FND-BSX**	**ISE-ELI**	**ISE-EXP**	**ISE-BSX**
Constraints editor	√	√	√	√	√	√	√	√	√
Floorplanner	√	√	√	√	√	√	√	√	√
CPLD ChipViewer	√	√	√	√	√	√	√	√	√
Pin Editor	√	√	√	√	√	√	√	√	√
FPGA Editor	√	√	√	√	√	√	√	√	√
Core Generator included	√	√	√	√	√	√	√	√	√
Configuration by cable	√	√	√	√	√	√	√	√	√
Error navigation to Xilinx Web							√	√	√
Command line operation							√	√	√
HTML timing reports	√	√	√	√	√	√	√	√	√
Data Book I/O timing	√	√	√	√	√	√	√	√	√
Project archiving	√	√	√	√	√	√	√	√	√
System Interfaces									
EDIF in	√	√	√	√	√	√			
PROM file generation	√	√	√	√	√	√	√	√	√
JTAG download software	√	√	√	√	√	√	√	√	√
IBIS	√	√	√	√	√	√	√	√	√
STAMP	√	√	√	√	√	√	√	√	√
VHDL, Verilog	√	√	√	√	√	√	√	√	√
HDL Simulation libraries	√	√	√	√	√	√	√	√	√

*VSS - Delivered as part of the ALLSTAR program or as a backPACK module in WebPACK

Lead Product Device Support Comparison

		Alliance Series		Foundation Series				ISE Series		
Family	Part Number	ALI-STD	ALI-ELI	FND-EXP	FND-ELI	FND-BAS	FND-BSX	ISE-ELI	ISE-EXP	ISE-BSX
Virtex	XCV50 only					√	√			√
	All devices up to XCV1000	√	√	√	√			√	√	
Virtex-E	XCV50E only					√	√			√
	All devices up to XCV1000E	√	√	√	√			√	√	
	All devices up to XCV3200E		√		√			√		
Virtex-EM	XCV405EM	√	√	√	√			√	√	
	XCV812EM	√	√	√	√			√	√	
Spartan	XCSxx (All devices)	√	√	√	√	√	√	√	√	√
Spartan XL	XCSxxXL (All devices)	√	√	√	√	√	√	√	√	√
Spartan-II	XC2SxxXL (Includes XC2S200)	√	√	√	√	√	√	√	√	√
XC9500 Series	XC9500 XV/XL (All devices)	√	√	√	√	√	√	√	√	√
XC400 Series	XC4000E/L/EX (All devices)	√	√	√	√	√	√	√	√	√
	XC4000XL/XLA (All devices up to XC4020)					√	√			√
	XC4000XL/XLA (All devices)	√	√	√	√			√	√	
	XC4000XV (All devices)	√	√	√	√			√	√	
XC3000 Series	XC3x00A/L (All devices)	√	√	√	√	√	√			
XC5200 Series	XC5200 (All devices)	√	√	√	√	√	√			

***Note**: CoolRunner Series is only available in WebFITTER and WebPACK at this time.