Design a Low-Power SMBus System Using CoolRunner™ CPLDs

The ultra low-power CoolRunner CPLD is the ideal choice for SMBus systems, because you can easily configure it to suit your specific needs.

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Low-power devices use the System Management Bus (SMBus) protocol to communicate with components and peripherals. SMBus is a compatible derivative of the I²C two-wire serial bus protocol and can therefore reside in the same device. In addition to the I²C features, SMBus enhances systems designed for power management tasks. Because SMBus is often used in handheld devices containing "smart" batteries, CoolRunner CPLDs are the perfect solution for implementing the low-power SMBus components designed into these batteries.

A system that uses the SMBus protocol can pass information between components without the need for individual control lines. This passed information can contain manufacturer information, model numbers, part numbers, system status, control parameters, errors, and so on. SMBus is so flexible you can even add or remove components during system operation. It also has the ability to determine arbitration in multi-master systems, and if a newly inserted device has the ability to check packets of data for errors.

Functionality

The SMBus implementation for the CoolRunner CPLD consists of a microcontroller or microprocessor interface and an SMBus master/slave controller as shown in Figure 1. It implements the following features:

• Microcontroller interface.

• Master or slave operation.

• Multi-master operation.

• Host operation.

• Automatic mode switching between master and slave.

• Calling address identification.

• START and STOP signal generation and detection.

• Repeated START signal generation.

• Acknowledge bit generation and detection.

• Bus busy detection.

• From 10 to 100 kHz operation.

• Optional signal SMBSUS# for system suspend mode.

• Optional signal SMBALERT# for slave interrupt request.

• Packet Error Code (PEC) using 8th polynomial Cyclic Redundancy Check (CRC-8) methods.

• Automatic determination of PEC capable devices.

• Compliant with System Management Bus Specification Rev. 1.1. (Note: the new SMBUS 2.0 Specification was posted Aug. 3.

See http://www.smbus.org/index.html.)

• Software selectable SMBus acknowledge bit.

• Arbitration.

A more detailed description of the SMBus controller is shown in Figure 2. You can easily modify the microcontroller interface to adapt the design to any microcontroller of your choice.

This design was created in VHDL using Xilinx WebPACK™ ISE (Integrated Synthesis Environment). It was verified using ModelSim™ XE (Xilinx Edition) simulation software.

Conclusion

You can get started with your own CoolRunner CPLD SMBus design by visiting the Xilinx website at www.xilinx.com/xapp/xapp353.pdf. Download (for free) the following:

• Complete detailed application notes.

• Complete VHDL source code.

• VHDL test benches.

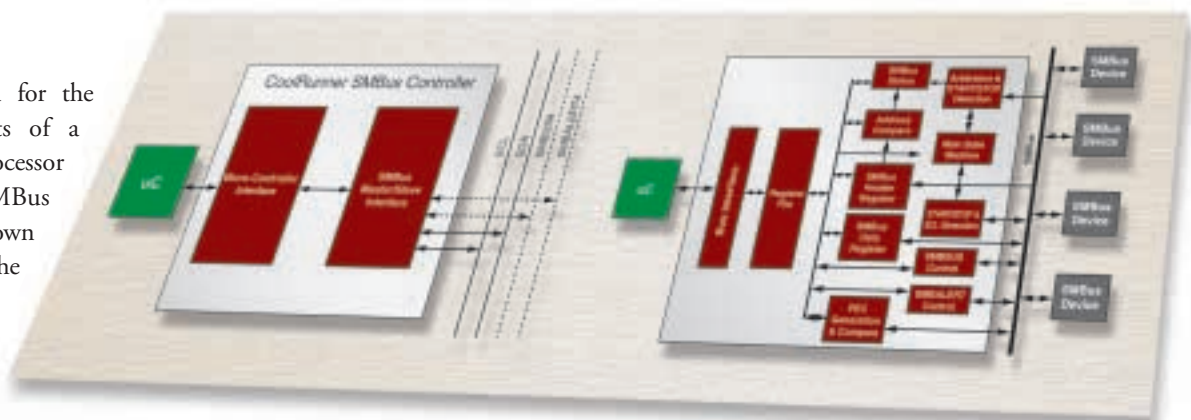*Figure 1 - Basic SMBus controller functions*

Figure 2 - SMBus controller detailed block diagram