Using In-System Programmability in Boundary-Scan Systems

XAPP070 July, 1997 (Version 1.1) Application Note

Summary

This application Note discusses basic design considerations for in-system programming of multiple XC9500 devices in a boundary-scan chain, and shows how to design systems that contain multiple XC9500 devices as well as other IEEE 1149.1-compatible devices.

Xilinx Family

XC9500

Introduction

The XC9500 family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. Xilinx also provides the EZTag™ software that automatically programs and tests XC9500 devices from the standard test vector and device programming files generated by most CPLD development tools.

XC9500 TAP Characteristics

The AC and DC characteristics of the XC9500 TAP are described as follows.

TAP Timing

Figure 1 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations. The timing for the INPUT-I/O-CLK and I/O signals is relevant to boundary-scan operations (such as EXTEST) that activate or strobe the system pins.

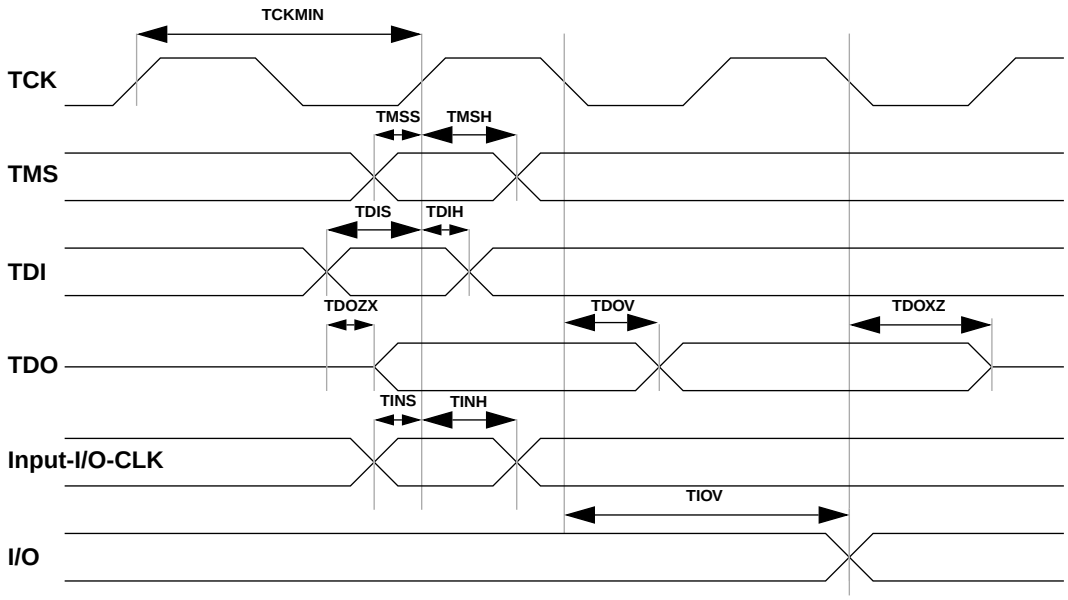

Figure 1: Test Access Port Timing

TAP AC Parameters

Table 1 shows the timing parameters for the TAP waveforms shown in Figure 1.

Table 1: Test Access Port Timing Parameters (ns)

Symbol	Parameter	Min	Max
TCKMIN	TCK Minimum Clock Period	100	
TMSS	TMS Setup Time	10	
TMSH	TMS Hold Time	10	
TDIS	TDI Setup Time	15	
TDIH	TDI Hold Time	25	
TDOZX	TDO Float to Valid Delay		35
TDOXZ	TDI Valid to Float Delay		35
TDOV	TDO Valid Delay		35
TINS	I/O Setup Time	15	
TINH	I/O Hold Time	30	
TIOV	EXTEST Output Valid Delay		55

Terminating TAP pins

The XC9500 TDI and TMS pins have internal 15Kohm pull-up resistors, which are required by the 1149.1 standard. Because these pins are internally terminated, no further termination is required on the TAP connections.

Capacitive Decoupling

Decouple the Vcc input with a 0.1 uF capacitor connected to the nearest ground plane (low inductance surface mount capacitors are recommended). Decouple the printed circuit board power inputs with 0.1 uF ceramic and 100 uF electrolytic capacitors. This helps to provide a stable, noise free power supply to the ISP parts.

Free Running Oscillators

Boundary-scan operations often involve the transmission of long streams of data through long and complex paths that traverse the entire system. Often, the presence of active clocks and free running oscillators will couple noise onto the boundary-scan chain TAP signals. To increase the reliability of boundary-scan and ISP operations, equip your system with a clock and oscillator disable. The disable should be activated for all test and program operations when using the download cable, ATE or third party systems.

Calculating Maximal Chain Lengths

The XC9500 TAP pins have approximately 5 pF of signal loading. Because each TDI input is driven by only one TDO output (or equivalent single drive) there are no signal limitations related to those connections beyond those of standard board interconnect design rules.

The maximum TDO frequency will be 1/2 of the maximum TCK frequency. Because TCK and TMS are parallel driven signals the maximum number of parts in a single boundary-scan chain is determined by the ability of the TCK and TMS drivers to deliver the signals at the appropriate frequencies to the parts in the boundary-scan chain. Standard board-layout design rules also apply here.

If the boundary-scan chain includes more than 6 devices, buffered distribution of TMS and TCK are recommended.

Part Enable Ordering

The ISPEX instruction allows the flexibility to enable parts in an arbitrary order. In some systems the order in which parts are enabled is critical. For instance, if a slave device awakens before its controller, it may enter an error condition from which it cannot exit.

The EZTag software enables each part immediately after programming. In concurrent mode the parts are enabled in order from system TDI to system TDO.

Creating Boundary-Scan Chains

There are a number of possibilities for creating boundary scan chains, several of which are discussed in the following sections

Single Port Serial Chain

The most simple and widely-used boundary-scan configuration is the single port serial chain shown in Figure 2, and only this type of configuration is supported by the EZTag software. In this configuration, four pins are allocated in the system to facilitate connection of the TCK (clock), TMS (mode), TDI (Test Data Input), and TDO (Test Data Output) signals.

All devices in the chain share the TCK and TMS signals. The system TDI signal is connected to the TDI input of the first device in the boundary-scan chain. The TDO signal from that first device is connected to the TDI input of the second device in the chain and so on. The last device in the chain has its TDO output connected to the system TDO pin.

Other more complex chain variations are discussed later in this application note. Software supplied by third party developers supports these complex chain configurations.

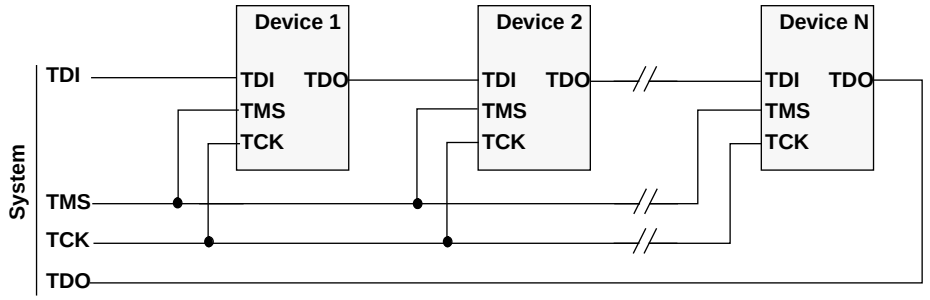

Figure 2: Single Port Serial Boundary-Scan Chain

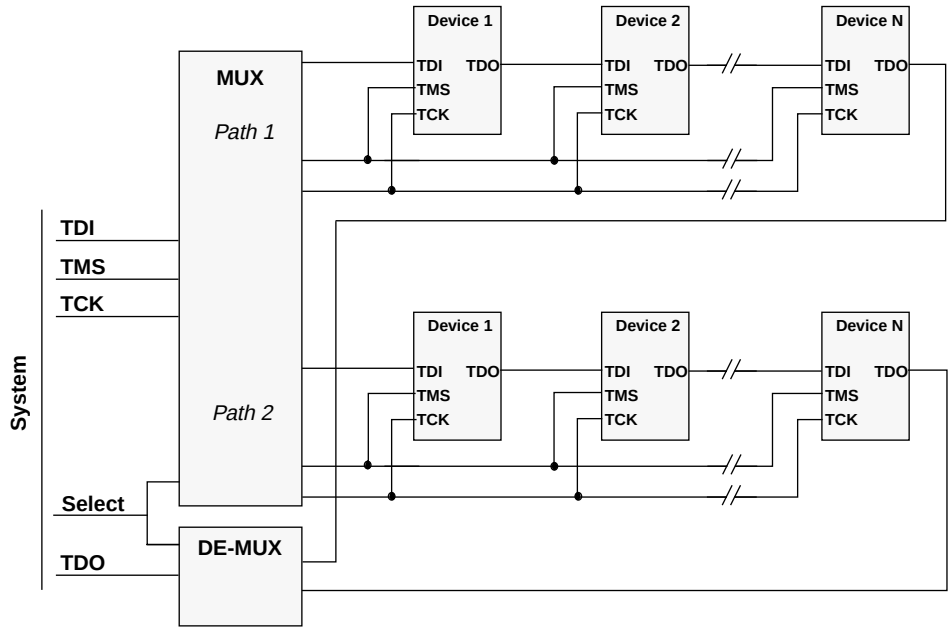

Figure 3: Star Configuration

Star Configuration

The single port serial chain, shown in Figure 3, configuration has a significant limitation due to the possibility that a defect in the backplane wiring or the removal of a board from the system will break the chain. This would make ISP and system testing impossible. In order to overcome this limitation and make the 1149.1 standard practical for very large systems, the standard allows the connection of boundary-scan chains in star configuration in which the four pins of the TAP are multiplexed. The costs of this approach are the additional overhead required to switch between scan paths, and the reduced TCK frequency due to TMS routing delays.

Multiple Independent Paths

In the topology shown in Figure 4, the TDI and TDO paths are independent allowing data to be streamed into and out of the portions of the system independently.

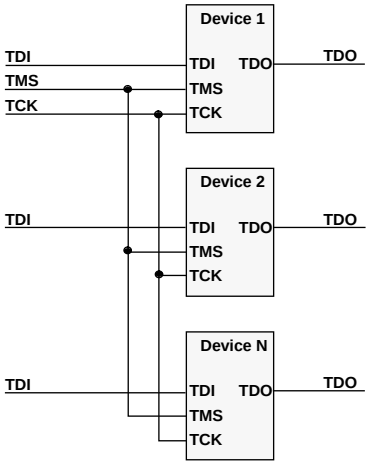

Figure 4: Multiple Independent Chains

Parallel Chains

In the topology shown in Figure 5, TDI and TMS inputs are independent but the TDO is shared. This means that although data can be streamed into portions of the system independently, data being streamed out is time multiplexed through TMS control.

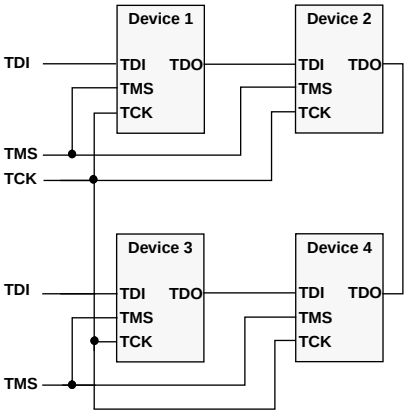

Figure 5: Parallel Chains

In-System Programming

Using the Xilinx Download Cables

The EZTag software can be used with either the Xilinx JTAG parallel download cable or the Xilinx serial XChecker cable.

IBM PC compatible systems can use the Xilinx high speed Parallel Cable III (part number DLC5). The cable pod includes port protection and drive circuitry which requires a 5V power supply that is usually is supplied by the target system. This cable operates TCK at a frequency of between 100KHz and 300Khz which is determined by the port speed of the host computer.

Sun and HP workstations (as well as IBM PC-compatible systems) use the Xilinx XChecker cable, which connects to the computer's serial port. The XChecker cable pod contains an XC3042 FPGA and 1Mbit of static RAM. The FPGA is configured to operate as a UART to facilitate host-cable communications. It also includes circuitry to enable high speed 1149.1 TAP signal processing the collecting TDO results in XChecker's static RAM. The TDO data can then be uploaded to the host. Like the parallel cable, the XChecker cable requires 5V to operate and this is usually provided by the target system.

When addressing the TAP the XChecker cable operates at TCK frequencies of approximately 1 MHz, which is controlled by a crystal in the XChecker cable pod. Although the cable TAP driver can operate at 1MHz, the overall speed of this cable is determined by the serial port throughput which is typically 38K baud.

The parallel and serial cable characteristics are:

- Power - A 5V power supply capable of providing 125 mA peak current and 60 mA steady state is required. The parallel cable requires a 5V power supply capable of providing 20 mA current.
- Drive Capabilities - The XChecker cable outputs are capable of sourcing or sinking up to 4 mA. The parallel cable outputs are capable of sourcing or sinking up to 20 mA.
- Special considerations - For both the XChecker and parallel download cables, the 1149.1 TAP drive electronics is in the cable pod. This should be taken into account when extending the signal reach from the pod to the system. When extending the cable from the port connection side, the drive capabilities of the host computer's port itself must be considered.

Concurrent Program and Erase Modes

One operating mode of the EZTag software performs concurrent erasing and programming. The advantage of this approach is speed; the overall programming time is dictated by the slowest part in the boundary-scan chain. Also, the total number of vectors required is optimized. The disadvantage of this approach is that the system must supply a peak operating current equal to that required by all parts being programmed or erased concurrently. For more information on how to use this feature in EZTag, please see the Xilinx *EZTag User's Guide*.

Note: although XC9500 parts can be programmed concurrently, the current EZTag software does not generate an SVF file that supports this operation. The current EZTag generates an SVF file that bypasses all parts except the one being programmed.

ISP Mode I/O Behavior

The functional pins of the device transition to a high-impedance state when ISP mode is entered using the ISPEN instruction. At the completion of an ISP programming or erase operation, the ISPEX instruction is executed. When leaving ISPEX mode (by shifting in an new boundary-scan instruction other than ISPEN), the device initializes to its programmed state; the functional pins take on their selected operations (input, output, or bidirectional) and the device registers take on their pre-selected initial values.

System-Level Design Issues

The normal operating mode of a system or a device in the system is known as mission mode which is different from test mode. When operating a device in boundary-scan test mode (such as when using either INTEST or EXTEST) as well as when performing ISP operations, the device is effectively disconnected from the overall system. When the operation is completed, the device is re-connected to the system. This can sometimes result in unpredictable system behavior. Additional discussion regarding this problem can be found in "The Boundary-Scan Handbook" by Ken Parker. Fortunately, the XC9500 family supplies two proprietary boundary-scan instructions that serve to alleviate this problem.

XC9500 Mission Mode Exit and Re-Entry Techniques

The XC9500 devices support two boundary-scan instructions that can be used to help alleviate the problems associated with exiting and re-entering mission mode. The instructions are ISPEN (ISP enable) and ISPEX (ISP exit).

- **ISPEN** - The ISPEN instruction is used at the beginning of every block of ISP operations that will attempt to access for alteration or read the device internal program memory (such as program, erase, verify, etc.). When the device is in ISPEN mode, the device I/O pins immediately enter a state in which they are floating with a weak pull-up resistor enabled on each pin. The device pins therefore neither drive nor sense external signal levels.
- **ISPEX** - The ISPEX instruction is used to conclude every block of ISP operations that have either been

read from or written to the device internal program memory. As long as the ISPEX instruction remains in the instruction register the functional pins remain in their lightly pulled-up high impedance state. Once the ISPEX instruction is replaced with any other boundary-scan instruction (except ISPEN), the device returns to its initial power state with the pins configured to their programmed states (input, output, or bidirectional) and with the device flip-flops taking on their initial states.

The ISPEX operation takes approximately 100 microseconds to complete. If the ISPEX instruction is held in the instruction register for longer than 100 microseconds, the ISPEX operation will not take effect until the ISPEX instruction is displaced from the instruction register.

In order to ensure safe operation, all INTEST,EXTEST, and ISP operations involving the XC9500 parts should be bracketed by ISPEN and ISPEX instructions.

The designer must also be careful to select an initial condition that is “system-safe” so that when the ISPEX instruction is released the XC9500 part in question will safely resume operation with the rest of the system.

Basic Boundary-Scan Design Guidelines

The following guidelines will help ensure a successful design.

- Make certain that all parts in the boundary-scan chain have 1149.1 compatible test access ports.
- Use simple buffering for TCK/TMS signals, to simplify test considerations for the boundary-scan TAP.
- Do not invert TCK or TMS pathways, to guarantee complete test software compatibility.
- Group similar device families, and have a single level converter interface between them, for TCK, TMS, TDI, TDO, and system pins.
- Check that the mission logic is safe from any possible errors that might arise while the boundary-scan data is being shifted through the boundary-scan chain. For example, pay close attention to bus enable or chip select signals that might be enabled simultaneously, causing unexpected bus contention.
- Provide the capability for the ATE to disable conventional (non boundary-scan) IC’s whose run-time node values might introduce conflicts with boundary-scan logic values during test operations.
- Verify that the entire system is held in a benign state during boundary-scan test operations.
- Verify that the set-up and hold times of TDI and TMS with respect to TCK are met by the system.

Debugging Boundary-Scan Systems

The following guidelines and helpful information will help isolate potential problems.

- When traversing the IR states, the CAPTURE-IR value specified in the BSDL file is always shifted out on TDO at SHIFT-IR. This fact can be used to test boundary-scan chain continuity.
- After exit from Test-Logic-Reset, if the system transitions directly to Shift-DR, the values shifted out on TDO must be either the IDCODE (if implemented) or the BYPASS register contents. If all logic 0’s are shifted in at TDI, then the first incidence of a logic 1 on TDO represents the first bit of an IDCODE. This fact can be used for blind interrogation of the boundary-scan chain and for further boundary-scan chain continuity checks.
- When entering ISP mode via the ISPEN instruction, all XC9500 function pins float to a weakly pulled-up high impedance state. The pins can easily be tested for this behavior.
- When ISPEX is shifted out of the instruction register, the XC9500 devices should take on their programmed values with the functional pins acting immediately as inputs or outputs, as programmed. The pins can easily be tested for this behavior.
- TDO assumes its defined value at the falling edge of TCK.
- When not in SHIFT-IR or SHIFT-DR, TDO exhibits high impedance.
- The last valid TDI bit clocks into the TAP with TMS high.
- In BYPASS mode, TDO equals the applied TDI data one TCK pulse earlier.

Conclusion

When designing ISP systems, common-sense rules related to electronic system design and board layout should be adhered to. In order to benefit from the synergies associated with the integration of test and programming operations the designer must consciously design with the entire system life cycle in mind.

References

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