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Powering Xilinx FPGAs

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Summary

Power consumption in Xilinx FPGAs depends upon the number of internal logic transitions and is proportional to the operating clock frequency. As device size increases, so does power consumption. It is common for a large, high-speed design to require several amperes of current. Without an accurate thermal analysis, the heat generated could easily exceed the maximum allowable junction temperature. Power supply requirements, including initial conditions, transient behavior, turn-on, and turn-off are also important. Bypassing or decoupling the power supplies at the device, in the context of the device's application, requires careful attention. All these aspects of the power supply must be considered in order to achieve successful designs.

Introduction

The power consumed in a Xilinx device is highly dependent on the design. Accurate power estimation methods must be used to ensure that a system power supply meets the FPGA's requirements. Thermal planning (to keep the die temperature within operational limits) and the design of power filtering networks also require accurate power data. This application note covers the following topics with regard to Virtex™, Virtex-E, Virtex-II, and Spartan™-II FPGAs:

- Estimation of the power requirements using the Virtex Power Estimator
- Thermal considerations with respect to ambient and junction temperatures
- Power supply requirements including initial conditions, transient behavior, turn-on, and turn-off
- Bypassing or decoupling the power supplies at the device

Power Requirements

To facilitate determining the power needs for a given design, Xilinx has created the Virtex Power Estimator, available at **http://www.xilinx.com/support/techsup/powerest/** on the Web. The instruction manual is published as **XAPP152, *Virtex Power Estimator Users Guide***, available at **http://www.xilinx.com/xapp/xapp152.pdf**. The Virtex Power Estimator worksheet estimates the power consumption for a Virtex design. The Spartan-II family employs the same architecture as the Virtex series. When using the Virtex Power Estimator for a Spartan-II device, simply select a Virtex device with the same density. To generate upper bound estimates for the XC2S15 and XC2S30, select the XCV50. Choose a similar menu option to match with the area and package type (CS, FG, PQ, or TQ). The worksheet considers the design resource usage, toggle rates, I/O power, and many other factors for an accurate estimation.

The formulas used in the program are based upon actual test design measurements, and values obtained from the Virtex Power Estimator are therefore *typical* results. An accurate computation of dynamic power consumption is only possible when the switching frequency of each node is known. Such detailed knowledge is only possible if the system behavior is taken into account.

Thermal Considerations

Four factors determine the temperature of an FPGA die: total power dissipation, package thermal resistance, ambient temperature, and airflow. These factors must be managed to stay below the maximum junction temperature of the die. The designer usually has control over at least one of these factors. If it is determined by thermal analysis that the die will exceed its

maximum temperature limits, the designer may choose to reduce the clock speed, improve airflow, change the package, or add a heatsink.

Given the temperature inside the case or rack (T_{AMB}), the total power dissipation of the FPGA (P) and the thermal resistance of the package (Θ_{JA}), the junction temperature (T_J) may be calculated.

$$T_J = T_{AMB} + P(\Theta_{JA}) \hspace{3cm} (1)$$

This equation shows that the die will experience a higher temperature than the ambient temperature. The total power dissipation (P), multiplied by the thermal resistance of the package (Θ_{JA}), is the difference between junction and ambient temperature.

The goal of thermal planning is to keep the die temperature below the maximum rated value. For commercial grade parts, the maximum value is 80 °C; for industrial grade, 100 °C. Exceeding this temperature will result in a degradation of performance; timing values in the datasheet will no longer be guaranteed. For both commercial and industrial grade parts, there is an absolute maximum temperature rating of 125 °C. If this temperature is exceeded, device reliability will be compromised.

As an example of the thermal analysis procedure, an average design in a V1000E is considered. The design runs at 75 MHz with 90% device utilization. These specifications yield a power dissipation value of five watts from the Xilinx **Power Estimator**. In a BG560 package, this leads to a die temperature 50°C higher than the ambient temperature. If the maximum ambient temperature in the application were 40°C (temperature inside the case or rack), the die would be at 90°C, exceeding the maximum temperature for a commercial grade device. These numbers are calculated using Equation 1 above:

P = 5 Watts
Θ_{JA} = 10.0°C/Watt (from chapter 8, table 3 of the 2000 data book)
T_{AMB} = 40°C
T_J = 40°C + 5 Watts x (10.0°C/Watt) = 90°C

This 50°C rise over ambient was with a bare package in still air. With a fan supplying 250 linear feet per minute (LFM) of air to the top of the package, the value for package thermal resistance drops to 7°C/W, bringing the die temperature to 75°C. With 500 LFM, the die temperature drops to 70°C. If fans are undesirable, a heatsink may also be used to decrease the effective thermal resistance from the die to the environment.

Power Supply Requirements

At power-up, the maximum V_{CCINT} rise time must remain less than 50 ms (reference the datasheets). The duration of the V_{CCINT} ramp will depend on the amount of current available from the power supply. If a large amount of current is available, the $V_{CC\ INT}$ ramp will be very fast. When the final voltage has been reached, this high current is no longer required. Likewise, if the available current is limited, the rise time will be lengthened. The rise should not be inhibited by a current trip, or current foldback. Current limit behavior is acceptable based on the "Power-On Ramp Up Current Requirement," specification from the data sheet. The voltage rise should be roughly monotonic. Dwelling at a voltage, or having a "plateau", is not acceptable power supply behavior. Having the voltage go up over the minimum operating voltage and then drop below this value may also result in incorrect power-on behavior. When the power supply voltage falls below the absolute minimum operating voltage when turned off, it should not rise immediately back to the nominal operating voltage without first discharging back down below 0.1 V DC. A resistor may be required to bleed off charge on the filter and bypass capacitors to insure this condition is met.

Power supplies for high-performance designs may be required to provide up to five amperes per device. These supplies must take into consideration the resistive drop encountered in the distribution of the power to the device. The dynamic performance will suffer if the IR drop causes the voltage at the device to be less than nominal.

For designs with a high clock speed and forced cooling, the resistive voltage drop may become significant. An increase in the V_{CCINT} and V_{CCIO} power supply voltage may be required to compensate for the resistive drop.

Some designs do not require as much power. Designs using very low toggle rates or small portions of logic have less dynamic power requirements. In these cases, the determining factor in power supply requirements is the startup and configuration current for the chosen device. The DC characteristic section of the datasheet has quiescent and configuration current ratings for each device.

Bypassing Considerations

With high-speed, high-density FPGA devices, maintaining signal integrity is key to reliable, repeatable designs. Proper power bypassing and decoupling improves the overall signal integrity. Without it, power and ground voltages are affected by logic transitions and can cause operational issues.

When a logic device switches from a logic one to a logic zero, or a logic zero to a logic one, the output structure is momentarily at a low impedance across the power supply. Each transition requires that a signal line be charged or discharged, which requires energy. As a result, a lot of electrons are suddenly needed to keep the voltage from collapsing. The function of the bypass capacitor is to provide local energy storage.

This local energy storage must be available over a broad frequency range. Very small capacitors with low series inductance are used to provide fast current for the high frequency transitions. Larger, slower capacitors continue to supply current after the high-frequency capacitors energy is expended. Current FPGA technology requires capacitance in three frequency ranges, referred to as high, medium, and low. These frequencies span from the 1 KHz range to the 500 MHz range—the switching knee frequency. The knee frequency is related to the edge rates of logic transitions and may be approximated by taking the reciprocal of twice the signal rise time. For further discussion, see Johnson and Graham's book *High-Speed Digital Design*.

Proper placement is very important for high-frequency capacitors (0.1 μF to 0.001 μF low-inductance ceramic chip). It is less important for middle-frequency capacitors (47 μF to 100 μF tantalum), and even less important for low-frequency capacitors (470 μF to 3300 μF).

The reason for this dependence on placement is simple: Inductance in the path from capacitor terminals to the FPGA power pins must be kept as low as possible. This means keeping the path as short as possible, even when the path is through a solid ground or power plane. All distances are significant since the inductance of one inch of solid copper plane is about 1 nH. Bypass capacitor vias must travel straight down to the ground or V_{CC} plane.

High-frequency bypass capacitors, whether on V_{CCINT} or V_{CCIO}, should be mounted within one centimeter of the associated V_{CC} pin. In most cases, satisfying this requirement means mounting the capacitors on the underside of the PCB, underneath the FPGA. If this is not possible, the capacitors should be mounted as close as possible around the periphery of the device.

Middle-frequency bypass capacitors for V_{CCINT} and V_{CCIO} should be mounted within three centimeters of the V_{CC} pins. Again, the underside of the board is the best place to mount these.

Low-frequency bypass capacitors may be mounted anywhere on the board, within reason. Of course, the closer they are to the FPGA(s), the better. Some designs may omit capacitors of this size if large amounts of low-frequency energy are not required. If this requirement cannot be established with a reasonable amount of certainty (e.g., simulation of the entire power system), the low-frequency capacitors should be included—and most designs will require them in any case.

Core V_{CC} Bypass Calculation

The core of a Xilinx FPGA has a requirement for some very small, short-duration (< 50 ps) currents. Combining these currents across the whole device can add up to amperes of current.

Since the individual switches are numerous, core bypassing design is approached with an average energy storage requirement. This method gives a conservative estimate of bypass capacitor requirements, so typical power estimates (rather than worst case) should be used.

A fundamental equation (Equation 2) is used to determine the requirement for high-frequency capacitors.

$$P = CV^2F \qquad (2)$$

Solving for C gives an equation for the equivalent capacitance of the FPGA (C_{EQ}) as a function of the core power (P), the core voltage (V), and the clock frequency (F).

$$C_{EQ} = \frac{P}{V^2F} \qquad (3)$$

C_{EQ} represents the equivalent switched capacitance of the entire FPGA. This value allows a choice of the optimum size high frequency bypass capacitors. In order to keep the V_{CCINT} variation (noise) small, the bypass capacitance must be much larger than the FPGA equivalent capacitance. The high-frequency bypass capacitance (C_{BT}) should be a factor of 25 to 100 times bigger than the FPGA equivalent capacitance (C_{EQ}). A factor (S) of 25 will result in one twenty-fifth, or a 4% variation in V_{CCINT}. Similarly, a factor of 100 results in a 1% variation in V_{CCINT}. Completing our example with a scale factor of 50 (for 2% variation) gives:

$$C_{BT} = (S \times C_{EQ}) \qquad (4)$$

Every V_{CCINT}/GND pair should have a high-frequency bypass capacitor. To determine the optimum size of each capacitor (C_{BI}), divide the total C_{BT} by the number of V_{CCINT} pins on the device, and round up to the next commonly available value.

$$C_{BI} = \frac{C_{BT}}{N_P} \qquad (5)$$

Combining equations gives an expression for the minimum size of each high-frequency V_{CCINT} capacitor (C_{BI}):

$$C_{BI} = \frac{C_{BT}}{N_P} = \frac{S \times C_{EQ}}{N_P} = \frac{S \times \dfrac{P}{V^2F}}{N_P} \qquad (6)$$

As an example, consider an XCV1000E in a BG560 package running at 75 MHz and dissipating five watts. The variation in V_{CCINT} should be no more than 2%, which corresponds to a scale factor of 50. The BG560 package has 36 V_{CCINT} pins, giving the value for N_P

P = 5 Watts
V = V_{CCINT} = 1.8 V
F = 75 MHz
S = 50
N_P = 36

$$C_{BI} = \frac{50 \times \dfrac{5W}{(1.8V)^2 \times 75MHz}}{36} = 0.028 \mu F$$

The minimum size for each high-frequency capacitor is 0.028 µF. The next larger available capacitor size should be chosen (0.047 µF or 0.1 µF).

With the high-frequency bypass capacitors determined, the medium- and low-frequency capacitors are chosen next. Tantalum capacitors from 47 µF to 100 µF are appropriate for the middle frequency range. If tantalum is not available, a low-inductance aluminum electrolytic

type may be used. The device requires at least one mid-frequency capacitor for every 1500 CLBs in the device. This means a V1000E should have at least four mid-frequency capacitors mounted within 3 cm of the device.

At least one low-frequency capacitor (470 μF to 3,300 μF) for every four FPGAs may be mounted anywhere on the board.

I/O Power Supply Bypass Calculation

With the large number of input/output structures now available on a single device, care must be taken to provide adequate bypassing to the V_{CCO} power supply pins. Like V_{CCINT}, I/O bypass requirements are calculated based on an average energy storage requirement. Here, it is the loads driven by the FPGA that determine the size of the equivalent switched capacitance. Since different I/O banks often operate at different voltages, their bypassing networks should be designed independently.

To determine the equivalent capacitance (C_{EQ}) of the loads associated with one bank or one voltage level, the number of loads (N_L) is multiplied by the value of the load (C_L).

$$C_{EQ} = (N_L \times C_L) \tag{7}$$

To keep the variation (noise) in V_{CCO} small, the bypass capacitance must be much larger than the equivalent load capacitance. The high-frequency bypass capacitance should be 25 to 100 times larger than the equivalent load capacitance. Equation 4 is used to calculate the total high-frequency bypass capacitance (C_{BT}).

Every V_{CCO}/GND pair should have a high-frequency bypass capacitor. To determine the optimum size of each capacitor (C_{BI}), divide the total C_{BT} by the number of V_{CCO} pins in the bank (N_P), and round up to the next commonly available value. Equation 8 results from combining equations to produce an expression for the minimum size of each high-frequency V_{CCO} capacitor C_{BI} .

$$C_{BI} = \frac{C_{BT}}{N_P} = \frac{S \times C_{EQ}}{N_P} = \frac{S \times N_L \times C_L}{N_P} \tag{8}$$

Continuing the XCV1000E example, assume the design has 40 outputs in an I/O bank. Each load is 10 pF. The BG560 package has five V_{CCO} pins in each bank, and the maximum V_{CCO} variation is to be 2%.

S = 50
N_L = 40
C_L = 10 pF
N_P = 5

$$C_{BI} = \frac{50 \times 40 \times 10\text{pF}}{5} = 0.004\,\mu\text{F} \tag{9}$$

The minimum size for each high-frequency capacitor is 0.004 μF. The next larger available capacitor size should be chosen (0.0047 μF or 0.01 μF).

There should be one middle-frequency capacitor of value 47 μF to 100 μF for every one to four V_{CCO} banks. Tantalum capacitors are appropriate for the middle frequency range. If tantalum is not available, a low-inductance aluminum electrolytic type may be used. These capacitors should be mounted within three centimeters of the V_{CCO} pins.

At least one low-frequency capacitor (470 μF to 3,300 μF), should be used for each voltage level. One capacitor can be used for up to four devices.

Capacitor Characteristics

Because of the input/output bypassing requirements of newer devices, capacitor types formerly used in lower speed or lower density designs may not be effective. Bypass capacitors, depending on their material, construction, and value, have different series reactances over

frequency. By examining the data sheets for the various families, (i.e., X7R, Z5U), it becomes apparent that some are better suited for the application under consideration.

Impedance variation with frequency is shown in Figure 1. As an example, an industry-standard type X7R monolithic 0.01 μF ceramic 1206 chip capacitor has an impedance of 0.2 Ω at 50 MHz. However, at 500 MHz, the impedance of the same capacitor is 3.0 Ω. The capacitor is ineffective when the energy stored is unavailable to the load due to the increase in effective impedance.

Temperature range must also be considered. Some capacitors have a low impedance at room temperature, but may perform poorly at temperature extremes. Z5U capacitors may have lower ESR at high frequencies for large value capacitors (0.1 μF to 0.33 μF). However, they are not recommended for use below 10°C. As +20%, –80% rated parts, they require almost double the design value to be safe. It is best to consult the capacitor manufacturer's data sheets in the selection of a bypass capacitor series.
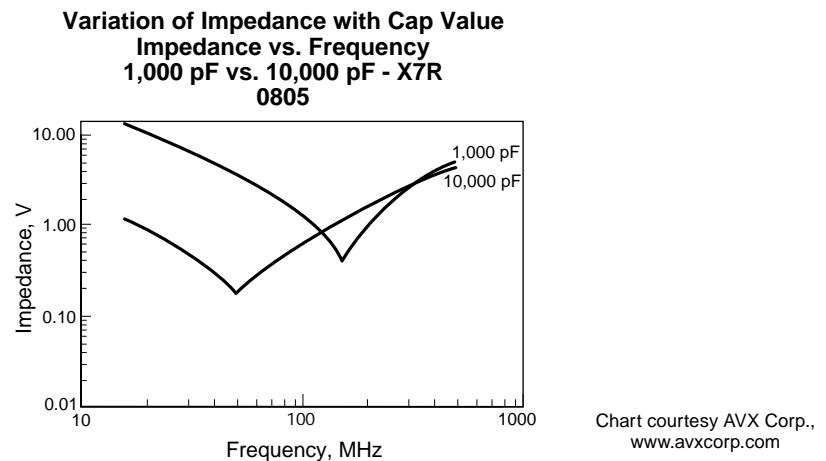
Variation of Impedance with Cap Value
Impedance vs. Frequency
1,000 pF vs. 10,000 pF - X7R
0805

Chart courtesy AVX Corp.,
www.avxcorp.com

Figure 1: **Capacitor Impedance vs. Frequency**

References

Howard Johnson and Martin Graham, *High Speed Digital Design: A Handbook of Black Magic,* Prentice Hall, New Jersey, 1993.

Conclusion

By considering the power consumption and thermal plan of a specific design, the device power supply requirements and proper power bypassing, stable and reliable systems can be easily developed. This application note applies to all devices in the Virtex, Virtex-E, Virtex-II and Spartan-II families.

Revision History

Date	Version #	Revision
09/28/99	1.0	Initial release.
11/15/99	1.1	Minor revisions and reformatted to new style.
09/26/00	1.2	Revisions to text and equations in each section.
10/04/00	1.3	Minor text revisions.
02/06/01	1.4	Addition of Virtex-II and Spartan-II device information.

Xilinx : Support : Design : Power Estimator

Virtex and Virtex-E Power Estimator

User License Xilinx Software License Agreement for using the Power Estimator. If you accept these license terms you may use the worksheet.

User Guide Virtex Power Estimator User Guide

Online Worksheet Virtex and Virtex-E Power Estimator for the Web

Standalone Worksheet Virtex Power Estimator V1.5 Excel'97 Spreadsheet.

- Due to French encryption policies Windows users with the French (Standard) regional setting will not be able to use the spreadsheet. For further information see the Microsoft Support Record documenting this issue.

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