Quad DataRate (QDR) SRAM Interface for Virtex-II Devices

XAPP262 (v1.0) January 15, 2001

Summary

The Virtex™-II family of FPGAs provides access to a variety of on-chip and off-chip RAM resources. In addition to the on-chip distributed RAM and block RAM features, Virtex-II FPGAs interface to a variety of external high-speed memory devices. The combination of the high-speed SelectI/O resources and on-chip Digital Clock Manager (DCM) circuits enables a high-bandwidth interface to Quad DataRate (QDR) architecture SRAMs. This application note describes the implementation of an interface using the Cypress CY17C1302V25 QDR SRAM.

Introduction

Specialized memory devices are needed to meet the requirements of high-performance data processing systems. By making conventional memory devices faster and optimizing memory bandwidth for a specific system architecture, overall performance is increasing in a variety of data processing systems. Examples of specialized memory products include dual-port memories, FIFOs, and CAMs.

The QDR SRAM architecture is one such evolution. Departing from the conventional memory architecture, QDR SRAMs provide two separate memory-access ports: a read port, and a write port. Both ports operate independently and allow simultaneous reads and writes into memory. Using established Double DataRate (DDR) technology accelerates the through put of each port, resulting in a quadrupling of memory bandwidth. Since the ports are separated, the problems associated with conventional bidirectional read/write ports (including bus turnaround) are avoided. This application note presents a general-purpose interface to a Cypress Semiconductor QDR SRAM device implemented in a Virtex-II XC2V250 device and operating at 166 MHz.

QDR SRAM Architecture

The Cypress semiconductor QDR SRAM (CY7C1302V25) is a 2.5 V, synchronous pipelined, 9 Mb SRAM organized as 256K words of 36 bits (Figure 1).

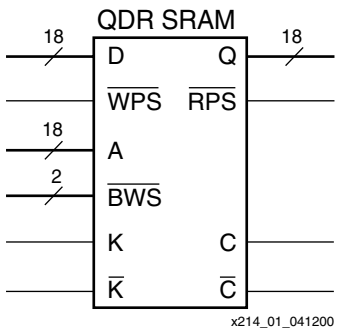

Figure 1: **Cypress QDR SRAM**

The Cypress device provides two independent memory access ports; one for read access, one for write access, on a common 18-bit address bus. Two control signals, Read Port Select ($\overline{RPS}$) and Write Port Select ($\overline{WPS}$), control activity on the two ports.

The device is internally organized as a 36-bit memory with 18-bit read and write data ports, where individual memory access always involves the exchange of two 18-bit data words. Writes

may involve all 36 bits or any combination of 9-bit groups, depending on the two Byte Write Select ($\overline{BWS}$) control inputs.

The QDR SRAM monitors the addresses to which simultaneous reads and writes occur. If a match is detected, the data being written to memory is "forwarded" to the read port. In this manner, the most up-to-date data is always available to the read port, even during simultaneous read/writes.

The QDR SRAM uses a pair of differential clocks, one for the write and address ports (K and $\overline{K}$), and one for the read port (C and $\overline{C}$). The purpose of the read-port clock is to enable board level deskewing of data launched from several QDR SRAM devices. In this application note, a single QDR SRAM is used, and the device is operated in a single clock mode (both C and $\overline{C}$ tied to V_{DD}), where K and $\overline{K}$ control both read and write access.

QDR Read and Write Timing

Read and write to the QDR SRAM begins on the rising edge of the QDR SRAM clock, K. A memory read is initiated by asserting $\overline{RPS}$ and providing the desired read address at the A inputs. With the QDR SRAM in single-clock mode (as used throughout this application note), the first group of 18 bits from the selected memory location appears on the next riding clock edge at the Q outputs. The second group of 18 bits appears at the outputs on the following falling clock edge (Figure 2).

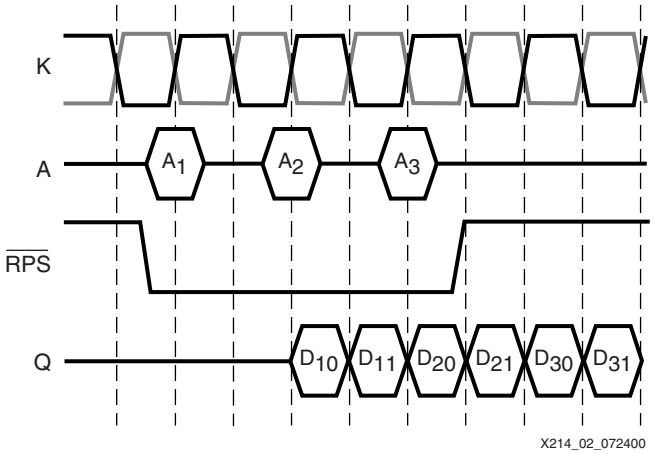

Figure 2: **QDR SRAM Read Access Timing**

A memory write is initiated by asserting $\overline{WPS}$ and providing the first group of 18 data bits at the D input. The falling edge of K is then used to latch the second group of 18 data bits at the D input and the address at the A input (Figure 3).

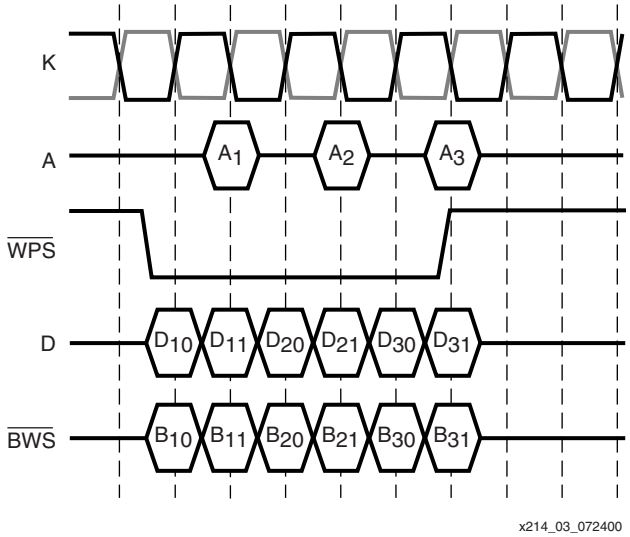

Figure 3: **QDR SRAM Write Access Timing**

Since the Q port is used only during a read and the D ports are used only during writes the read and write access may overlap. The shared address bus (A) is time-multiplexed with read addresses being latched on the rising clock (K) edge, and write addresses captured on the falling edge.

During write access, 18-bit write data may be divided into two 9-bit groups under the control of the $\overline{BWS}$ control inputs. Asserting $\overline{BWS}$ (0) permits the lower 9 bits [8:0] of data to be written to memory.

The Interface

A functional block diagram of the QDR SRAM interface is shown in Figure 4. When initiated on every clock cycle of the 166 MHz system clock the memory access is triggered by asserting the appropriate command ($\overline{CMD}$) input code. Descriptions of the command codes are listed in Table 1.

Table 1: **Interface command code**

CMD[1:0]	Function
11	No Operation
10	Read Access
01	Write Access
00	Simultaneous Read and Write

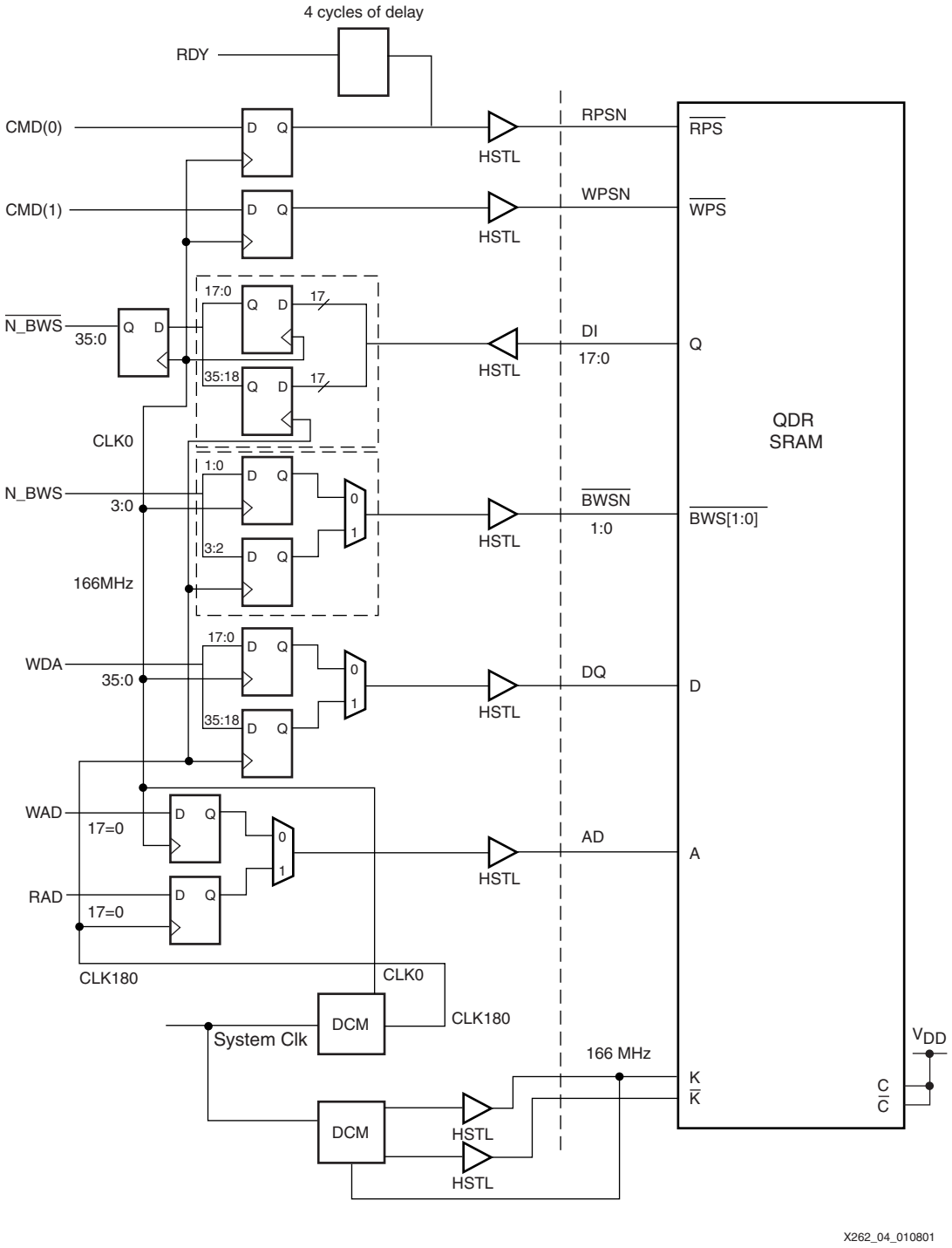

Figure 4: **Functional Block Diagram**

Write Datapath

On the input side, the write-request input $\overline{\text{CMD}}$ [1] is asserted, and an 18-bit write address (WAD), 4-bit $\overline{\text{BWS}}$ word, and 36-bit data (WDA) are presented to the interface. The data is separated into two 18-bit words before being communicated to the QDR SRAM at 166 Mhz. The address is similarly communicated to the SRAM, but is first interleaved with any memory-read accesses taking place.

During memory writes, 9-bit groups are individually masked, preserving the corresponding bits in memory. The four active-low $\overline{BWS}$ inputs are linked to 9-bit groups as shown in Table 2. Deasserting all four $\overline{BWS}$ inputs effectively cancels the write operation.

Table 2: Relationship between $\overline{BWS}$ and WDA bits

$\overline{BWS}$ [0]	WDA [8:0]
$\overline{BWS}$ [1]	WDA [17:9]
$\overline{BWS}$ [2]	WDA [26:18]
$\overline{BWS}$ [3]	WDA [35:27]

Read Datapath

On the input side, an 18-bit read address is presented to the interface and the read-request input $\overline{CMD}$[0] is asserted. The read access is interleaved with any current memory-write accesses. Both 18-bit data words from the QDR SRAM at 166 MHz are received and reformatted by the interface into the intended 36-bit word width.

Since the reformatting process and QDR SRAMs memory access cycle are both pipelined, four system-clock cycles are consumed before the requested data is available. The interface indicates the availability of data by asserting its ready output $\overline{RDY}$.

Memory read, write, and simultaneous read/write cycles are illustrated in Figure 5.

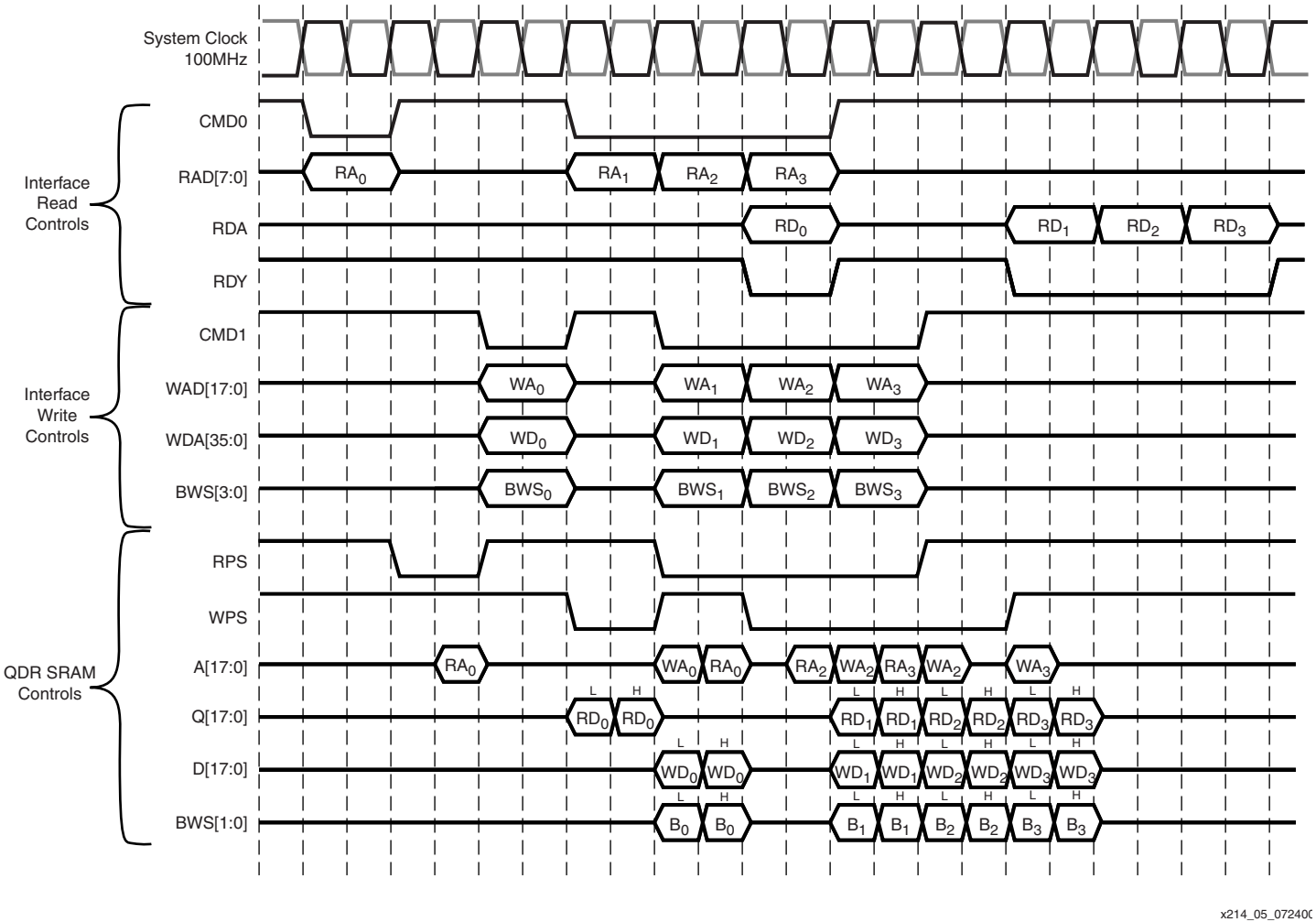

Figure 5: **Timing Waveforms Showing Read, Write and Simultaneous Read/Write Memory Access**

Functional Description

As shown in the Figure 4 block diagram, data is exchanged between the FPGA and the QDR SRAM on both rising edge and falling edge of K, the memory clock. Virtex-II devices have Double DataRate Registers (DDR) in the I/Os, significantly simplifying the interface between the FPGA and the QDR SRAM. The on-chip DCM generates the 166 Mhz and a 180° out-of-phase version of 166 MHz of the clock. These two clocks go to the clock pins of the input and output DDR registers. The use of DCMs ensures that the external 166 MHz and internal 166 MHz clocks are precisely phase locked with the source system clock.

All DDR communication between the FPGA and the QDR SRAM is implemented using the DDR registers in the FPGA I/O blocks.

During memory writes, the 36-bit write data and accompanying 4-bit $\overline{BWS}$ words are divided into two 18-bit words and two 2-bit words respectively. The lower-order bits are sent into the DDR register inputs that are controlled by CLK0. The higher-order bits are sent into the DDR input controlled by CLK180. The outputs of the DDR registers are then forwarded to the QDR SRAM.

Similarly, the 18-bit read and write addresses are sent to the DDR registers. The write address is selected by CLK0, and the read address is selected by CLK180.

During memory reads, the QDR SRAM launches 18-bit data on both the rising and falling edges of the 166 MHz memory clock, K. Data is captured at the FPGA by input DDR registers clocked at 166 MHz. The two 18-bits words from the DDR registers combine to form a single 36-bit word.

Reference Design

The VHDL interface reference design is available on the Xilinx web (**xapp262.zip** or **xapp262.tar.gz**). The Cypress QDR SRAM datasheet can be found on the **www.cypress.com** web site.

Implementation Notes:

The design is synthesized with Leonardo Spectrum 2001b.98. It is implemented in the Alliance 3.3I software tools. The system clock is deskewed by two DCMs. One DCM drives all the internal clocks inside the Virtex-II device; the other DCM is used to deskew the board.

To ensure that all the flip-flops are inside the I/Os, use a **-pr 0** option in MAP. To enable this option in the implementation GUI, go to the Implementation/Optimize and MAP template. Select the Map option = Pack I/O registers into IOB for the outputs.

Conclusion

This reference design implements an interface between a Virtex-II device and the Cypress CY17C1302V25 QDR SRAM.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/15/01	1.0	Initial Xilinx release.