XC4000X Series High-Reliability Field Programmable Gate Arrays

November 12, 1997 (Version 1.0)

Advance Product Specification

XC4000X Series Features

- Available in military temperature range (-55 ^{o}C to 125 ^{o}C, T_C)
- XC4036XL and XC4062XL available in -3 speed
- XC4028EX available in -4 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 50 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA Sink Current Per XC4000X Output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs

Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000XL: High Performance Low-Voltage Versions of XC4000EX devices
- 5V tolerant I/Os on XC4000XL
- 0.35µ SRAM process for XC4000XL

Introduction

XC4000X Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000E and XC4000X Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing.

Table 1: XC4000X Series High Reliability Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XC4028EX	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256	PG299, CB228
XC4036XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	PG411, CB228
XC4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	PG475, CB228

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* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Ordering Information

Example: **XC4062XL-3PG475M**