XCR3032XL 32 Macrocell CPLD

DS023 (v1.2) April 11, 2001 **Advance Product Specification**

Features

- Lowest power 32 macrocell CPLD
- 5.0 ns pin-to-pin logic delays
- System frequencies up to 175 MHz
- 32 macrocells with 800 usable gates
- Available in small footprint packages
  - 48-ball CS BGA (36 user I/O pins)
  - 44-pin VQFP (36 user I/O)
  - 44-pin PLCC (36 user I/O)
- Optimized for 3.3V systems
  - Ultra-low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five layer metal EEPROM process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V supply voltage at industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

Description

The XCR3032XL is a 3.3V, 32-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of two function blocks provide 800 usable gates. Pin-to-pin propagation delays are 5.0 ns with a maximum system frequency of 175 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3032XL TotalCMOS CPLD (data taken with two up/down, loadable 16-bit counters at 3.3V, 25°C).

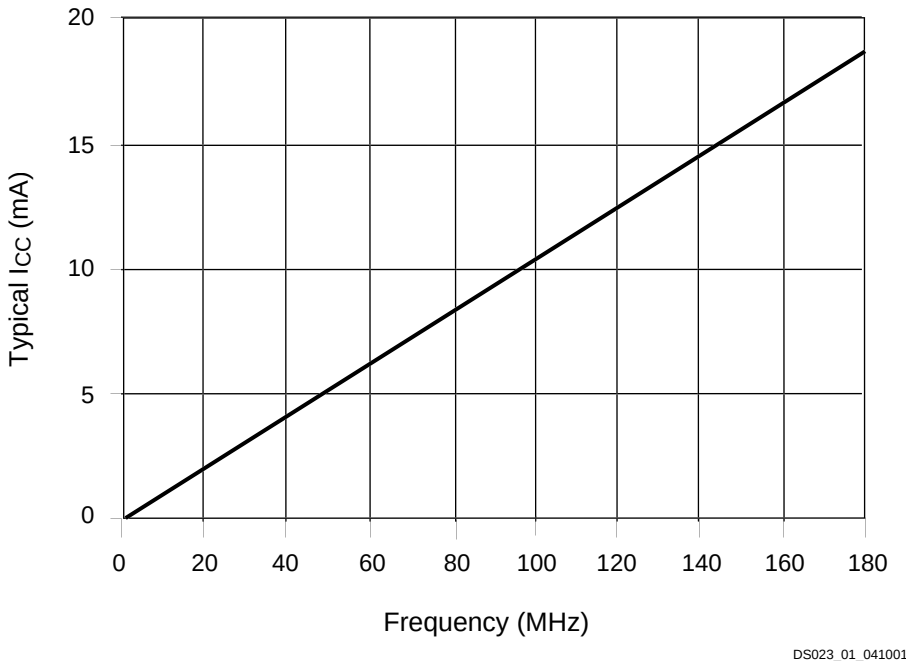


Figure 1: **I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **I_{CC} vs. Frequency** (V_{CC} = 3.3V, 25°C)

Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140	160	180
Typical I_{CC} (mA)	0.02	0.13	0.54	1.06	2.09	4.16	6.2	8.24	10.26	12.28	14.26	16.26	18.32

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}(2)	Output High voltage	V_{CC} = 3.0V to 3.6V, I_{OH} = –8 mA	2.4	-	V
		V_{CC} = 2.7V to 3.0V, I_{OH} = –8 mA	2.0(3)	-	V
		I_{OH} = –500 µA	90% V_{CC}	-	V
V_{OL}	Output Low voltage	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(4,5)	f = 1 MHz	-	TBD	mA
		f = 50 MHz	-	TBD	mA
C_{IN}	Input pin capacitance(6)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(6)	f = 1 MHz	-	12	pF
$C_{I/O}$	I/O pin capacitance(6)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (DS012) for recommended operating conditions
2. See Figure 2 for output drive characteristics of the XPLA3 family.
3. This parameter guaranteed by design and characterization, not by testing.
4. See Table 1, Figure 1 for typical values.
5. This parameter measured with a 16-bit, loadable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
6. Typical values, not tested.

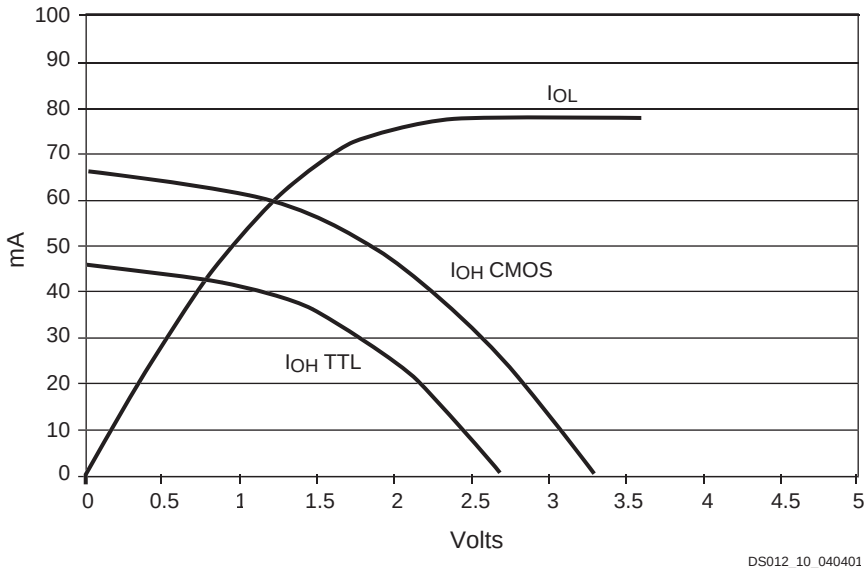


Figure 2: **Typical I/V Curve for the XPLA3 Family**

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-5		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)		4.5	-	7.0	-	9.1	ns
T_{PD2}	Propagation delay time (OR array)(3)		5.0	-	7.5	-	10.0	ns
T_{CO}	Clock to output (global synchronous pin clock)		3.5		5.0	-	6.5	ns
T_{SUF}(4)	Setup time fast	2.5	-	3.0	-	3.0	-	ns
T_{SU}(4)	Setup time	3.5	-	4.8	-	6.3	-	ns
T_{H}(4)	Hold time	0	-	0	-	0	-	ns
T_{WLH}(4)	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
Tt_{PLH}(4)	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T_{R}(4)	Input rise time	-	20	-	20	-	20	ns
T_{L}(4)	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}(4)	Maximum system frequency	-	175	-	119	-	95	MHz
T_{CONFIG}(4)	Configuration time(5)	-	20.0	-	20.0	-	20.0	µs
T_{POE}(4)	P-term OE to output enabled	-	7.2	-	9.3	-	11.2	ns
T_{POD}(4)	P-term OE to output disabled(6)	-	7.2	-	9.3	-	11.2	ns
T_{PCO}(4)	P-term clock to output	-	5.5	-	8.3	-	10.7	ns
T_{PAO}(4)	P-term set/reset to output valid	-	6.5	-	9.3	-	11.2	ns

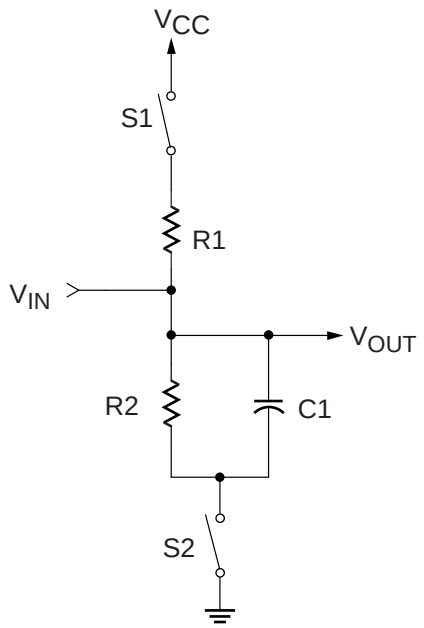
Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 4 for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 7 mA at 3.6V.
6. Output C_L = 5 pF.

Internal Timing Parameters(1,2)

Symbol	Parameter	-5		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	0.7	-	1.6	-	2.2	ns
T_{FIN}	Fast Input buffer delay	-	1.4	-	2.5	-	3.1	ns
T_{GCK}	Global Clock buffer delay	-	0.7	-	1.0	-	1.3	ns
T_{OUT}	Output buffer delay	-	1.8	-	2.7	-	3.6	ns
T_{EN}	Output buffer enable/disable delay	-	4.5	-	5.0	-	5.7	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	ns
T_{SUI}	Register setup time	1.0	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.0	-	2.3	-	2.1	ns
T_{RAI}	Register async. recovery	-	3.5	-	5.0	-	6.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	1.2	-	2.9	-	3.5	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	2.0	-	2.5	-	3.0	ns
T_{UDA}	Universal delay	-	1.0	-	2.0	-	2.5	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:
1. These parameters guaranteed by design and characterization, not testing.
2. See XPLA3 family data sheet (DS012) for timing model.

Switching Characteristics



Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

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Figure 3: **AC Load Circuit**

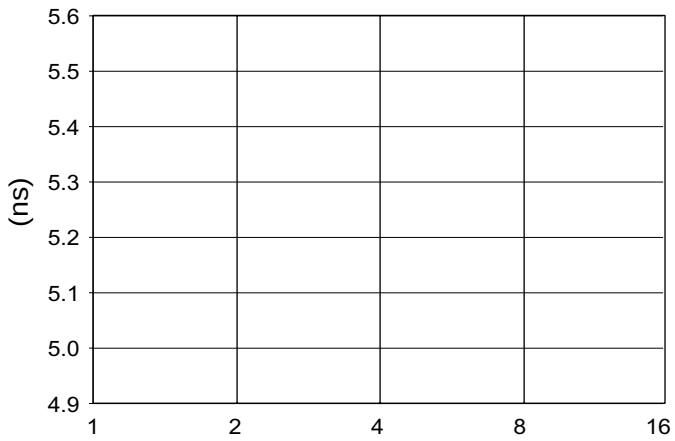

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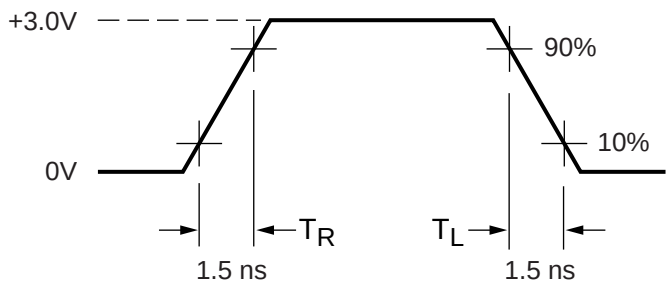
Figure 4: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

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Figure 5: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3032XL User I/O Pins**

	PC44	VQ44	CS48
Total User I/O Pins	36	36	36

Table 3: **XCR3032XL I/O Pins**

Function Block	Macrocell	PC44	VQ44	CS48
1	1	4	42	A2
1	2	5	43	A1
1	3	6	44	C4
1	4	7(1)	1(1)	B1(1)
1	5	8	2	C2
1	6	9	3	C1
1	7	11	5	D3
1	8	12	6	D1
1	9	13(1)	7(1)	D2(1)
1	10	14	8	E1
1	11	16	10	F1
1	12	17	11	G1
1	13	18	12	E4
1	14	19	13	F2
1	15	20	14	G2
1	16	21	15	F3
2	1	41	35	C5
2	2	40	34	A6
2	3	39	33	B6
2	4	38(1)	32(1)	B7(1)
2	5	37	31	D4
2	6	36	30	C6
2	7	34	28	D6
2	8	33	27	D7
2	9	32(1)	26(1)	E5(1)
2	10	31	25	E7
2	11	29	23	F7
2	12	28	22	G7
2	13	27	21	G6
2	14	26	20	F5

Table 3: **XCR3032XL I/O Pins**

Function Block	Macrocell	PC44	VQ44	CS48
2	15	25	19	G5
2	16	24	18	F4

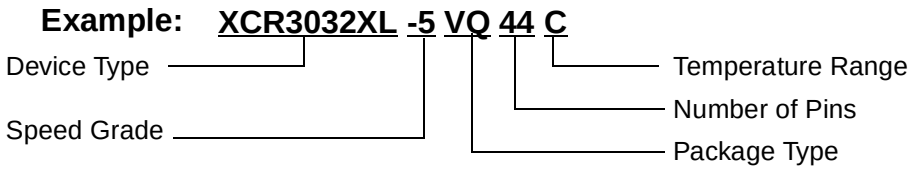
Notes:
1. JTAG pins

Table 4: **XCR3032XL Global, JTAG, Port Enable, Power, and No Connect Pins**

Pin Type	PC44	VQ44	CS48
IN0 / CLK0	2	40	A3
IN1 / CLK1	1	39	B4
IN2 / CLK2	44	38	A4
IN3 / CLK3	43	37	B5
TCK	32	26	E5
TDI	7	1	B1
TDO	38	32	B7
TMS	13	7	D2
PORT_EN	10(1)	4(1)	C3(1)
V_{CC}	3, 15, 23, 35	9, 17, 29, 41	B3, C7, E2, G4
GND	22, 30, 42	16, 24, 36	A5, E3, E6
No Connects	-	-	A7, B2, F6, G3

Notes:
1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet for full explanation.

Ordering Information



Device Ordering Options

Speed	
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay
-5	5 ns pin-to-pin delay

Package	
PC44	44-pin Plastic Lead Chip Carrier (PLCC)
VQ44	44-pin Very Thin Quad Flat Pack (VQFP)
CS48	48-ball Chip Scale Package

Temperature	
C = Commercial	T_A = 0°C to +70°C V_{CC} = 3.0V to 3.6V
I = Industrial	T_A = –40°C to +85°C V_{CC} = 2.7V to 3.6V

Component Availability

Pins		44	44	48
Type		Plastic PLCC	Plastic VQFP	Plastic BGA
Code		PC44	VQ44	CS48
XCR3032XL	-5	C	C	C
	-7	C,I	C,I	C,I
	-10	C	C	C

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/18/00	1.0	Initial Xilinx release.
02/05/01	1.1	Removed Timing Model.
04/11/01	1.2	Update TSUF spec to meet UMC characterization data. Added Icc vs. Freq. numbers, Table 1 and updated Figure 1. Added Typical I/V curve, Figure 2; added Table 2: Total User I/O; changed V_{OH} spec.