

Virtex-E Electrical Characteristics

Definition of Terms

The status of data sheets is designated as Preview, Advance, or Preliminary. These specifications are defined as follows:

Preview: These are rough estimates offered with the expectation that further refinements in accuracy are likely in subsequent revisions. These numbers are not guaranteed to be free of under-reporting.

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

All specifications are subject to change without notice.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description		Units
V _{CCINT}	Internal Supply voltage relative to GND	-0.5 to 2.0	V
V _{CCO}	Supply voltage relative to GND	-0.5 to 4.0	V
V _{REF}	Input Reference Voltage	-0.5 to 4.0	V
V _{IN}	Input voltage relative to GND	-0.5 to 4.0	V
V _{TS}	Voltage applied to 3-state output	-0.5 to 4.0	V
V _{CC}	Longest Supply Voltage Rise Time from 0 V – 1.71 V		ms
T _{STG}	Storage temperature (ambient)	-65 to +150	°C
T _{SOL}	Maximum soldering temp. (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T _J	Junction temperature	Plastic packages +125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- All user I/O is 3-stated prior to power-up. If the user I/O must remain in 3-state condition during power-up, V_{CCINT} must be applied prior to V_{CCO}.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V _{CCINT}	Internal Supply voltage relative to GND, T _J = 0 °C to +85°C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T _J = –40°C to +100°C	Industrial	1.8 – 5%	1.8 + 5%	V
V _{CCO}	Supply voltage relative to GND, T _J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T _J = –40°C to +100°C	Industrial	1.2	3.6	V
T _{IN}	Input signal transition time			250	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Description ¹	Device	Min	Max	Units
V _{DRINT}	Data Retention V _{CCINT} Voltage (below which configuration data might be lost)	All	1.5		V
V _{DRIO}	Data Retention V _{CCO} Voltage (below which configuration data might be lost)	All	1.2		V
I _{CCINTQ}	Quiescent V _{CCINT} supply current ¹	XCV405E		400	mA
		XCV812E		500	mA
I _{CCOQ}	Quiescent V _{CCO} supply current ¹	XCV405E		2	mA
		XCV812E		2	mA
I _L	Input or output leakage current	All	–10	+10	μA
C _{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
I _{RPU}	Pad pull-up (when selected) @ V _{in} = 0 V, V _{CCO} = 3.3 V (sample tested)	All	Note 2	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ V _{in} = 3.6 V (sample tested)		Note 2	0.25	mA

Notes:

- With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
- Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device¹ from 0 V. The fastest suggested ramp rate is 0 V to nominal voltage in 2 ms and the slowest allowed ramp rate is 0 V to nominal voltage in 50 ms.

Product (Commercial Grade)	Description ²	Current Requirement ³
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV1000E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	TBD
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:

- Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
- Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
- Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTTL (Note 1)	-0.5	0.8	2.0	3.6	0.4	2.4	24	-24
LVC MOS2	-0.5	0.7	1.7	2.7	0.4	1.9	12	-12
LVC MOS18	-0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	$V_{CCO} - 0.4$	8	-8
PCI, 3.3 V	-0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and \bar{Q}	V_{OH}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	1.25	1.425	1.6	V
Output Low Voltage for Q and \bar{Q}	V_{OL}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	0.9	1.075	1.25	V
Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and \bar{Q} signals	1.125	1.25	1.375	V
Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	2.2	V

Notes:

1. Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under **LVPECL**, with a 100 Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Virtex-E Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in “IOB Input Switching Characteristics Standard Adjustments” on page 6.

Description ¹	Symbol	Device	Speed Grade ²			Units	
			Min ³	-8	-7		-6
Propagation Delays							
Pad to I output, no delay	T_{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T_{IOPID}	XCV405E	0.51	1.0	1.0	1.0	ns, max
		XCV812E	0.55	1.1	1.1	1.1	ns, max
Propagation Delays							
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.75	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XCV405E	1.55	3.5	3.6	3.7	ns, max
		XCV812E	1.55	3.5	3.6	3.7	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T_{IOPICK} / T_{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	$T_{IOPICKD} / T_{IOICKPD}$	XCV405E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV812E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
ICE input	$T_{IOICECK} / T_{IOCKICE}$	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T_{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 2](#).
3. The numbers for Min are **Advance** product specification numbers.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade ¹				Units
			Min ²	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	-0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	-0.02	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	-0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	-0.05	-0.11	-0.11	-0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{IHSTL2}	SSTL2	-0.04	+0.04	+0.04	+0.04	ns
	T_{IHSTL3}	SSTL3	-0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	-0.03	+0.04	+0.04	+0.04	ns

Notes:

1. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 2](#).
2. The numbers for Min are **Advance** product specification numbers.

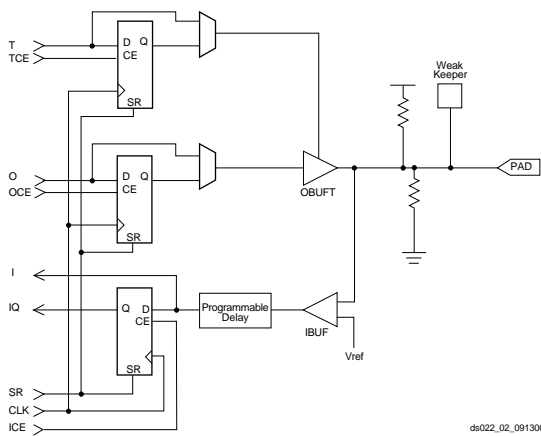


Figure 1: Virtex-E Input/Output Block (IOB)

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in “IOB Output Switching Characteristics Standard Adjustments” on page 8..

Description ¹	Symbol	Speed Grade ²				Units
		Min ³	-8	-7	-6	
Propagation Delays						
O input to Pad	T _{ILOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T _{ILOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T _{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T _{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	T _{IOTLPHZ}	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T _{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK to Pad	T _{ILOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T _{ILOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T _{ILOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T _{ILOCK / T_{ILOCKO}}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	T _{IIOCECK / T_{IIOCKOCE}}	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	T _{IIOSRCKO / T_{IIOCKOSR}}	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T _{IOTCK / T_{IIOCKT}}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	T _{IOTCECK / T_{IIOCKTCE}}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	T _{IIOSRCKT / T_{IIOCKTSR}}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T _{IIOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T _{IIOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T _{IIOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T _{IIOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.
3. The numbers for Min are **Advance** product specification numbers.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Description	Symbol	Standard	Speed Grade				Units
			Min ¹	-8	-7	-6	
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T _{OLVTTTL_S2}	LVTTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T _{OLVTTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T _{OLVTTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T _{OLVTTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T _{OLVTTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T _{OLVTTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T _{OLVTTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T _{OLVTTTL_F2}	LVTTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T _{OLVTTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T _{OLVTTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T _{OLVTTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T _{OLVTTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T _{OLVTTTL_F16}	16 mA	-0.10	-0.05	-0.05	-0.05	ns
	T _{OLVTTTL_F24}	24 mA	-0.10	-0.20	-0.20	-0.20	ns
	T _{OLVCMOS_2}	LVC MOS2	0.10	+0.09	+0.09	+0.09	ns
	T _{OLVCMOS_18}	LVC MOS18	0.10	+0.7	+0.7	+0.7	ns
	T _{OLVDS}	LVDS	-0.39	-1.2	-1.2	-1.2	ns
	T _{OLVPECL}	LVPECL	-0.20	-0.41	-0.41	-0.41	ns
	T _{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T _{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	-0.41	-0.41	-0.41	ns
	T _{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T _{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T _{OHSTL_I}	HSTL I	0.10	-0.51	-0.51	-0.51	ns
	T _{OHSTL_III}	HSTL III	-0.10	-0.91	-0.91	-0.91	ns
	T _{OHSTL_IV}	HSTL IV	-0.20	-1.01	-1.01	-1.01	ns
	T _{OSSTL2_I}	SSTL2 I	-0.10	-0.51	-0.51	-0.51	ns
	T _{OSSTL2_II}	SSTL2 II	-0.20	-0.91	-0.91	-0.91	ns
T _{OSSTL3_I}	SSTL3 I	-0.20	-0.51	-0.51	-0.51	ns	
T _{OSSTL3_II}	SSTL3 II	-0.30	-1.01	-1.01	-1.01	ns	
T _{OCTT}	CTT	0.0	-0.61	-0.61	-0.61	ns	
T _{OAGP}	AGP	-0.1	-0.91	-0.91	-0.91	ns	

Notes:

- The numbers for Min are **Advance** product specification numbers.

Calculation of $T_{i\text{oop}}$ as a Function of Capacitance

$T_{i\text{oop}}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{i\text{oop}}$ are based on the standard capacitive load (C_{sl}) for each I/O standard as listed in [Table 1](#).

Table 1: Constants for Use in Calculation of $T_{i\text{oop}}$

Standard	C_{sl} (pF)	fl (ns/pF)
LVTTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTTL Slow Slew Rate, 24mA drive	35	0.048
LVC MOS2	35	0.041
LVC MOS18	35	0.050
PCI 33 MHz 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

- I/O parameter measurements are made with the capacitance values shown above. See the [Application Examples](#) for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{i\text{oop}}$.

$$T_{i\text{oop}} = T_{i\text{oop}} + T_{\text{opadjust}} + (C_{\text{load}} - C_{sl}) * fl$$

where:

T_{opadjust} is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 2: Delay Measurement Methodology

Standard	V_L^1	V_H^1	Meas. Point	V_{REF} (Typ) ²
LVTTTL	0	3	1.4	-
LVC MOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I & II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I & II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	V_{REF}	Per AGP Spec
LVDS	$1.2 - 0.125$	$1.2 + 0.125$	1.2	
LVPECL	$1.6 - 0.3$	$1.6 + 0.3$	1.6	

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

I/O parameter measurements are made with the capacitance values shown in [Table 1](#). See the [Application Examples](#) for appropriate terminations.

I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min ¹	-8	-7	-6	
GCLK IOB and Buffer						
Global Clock PAD to output.	T _{GPIO}	0.38	0.7	0.7	0.7	ns, max
Global Clock Buffer I input to O output	T _{GIO}	0.11	0.19	0.45	0.50	ns, max

Notes:

- The numbers for Min are **Advance** product specification numbers.

I/O Standard Global Clock Input Adjustments

Description ¹	Symbol	Standard	Speed Grade				Units
			Min ²	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T _{GPLVTTL}	LVTTTL	0.0	0.0	0.0	0.0	ns, max
	T _{GPLVCMOS2}	LVCOS2	-0.02	0.0	0.0	0.0	ns, max
	T _{GPLVCMOS18}	LVCOS2	0.12	0.20	0.20	0.20	ns, max
	T _{GLVDS}	LVDS	0.23	0.38	0.38	0.38	ns, max
	T _{GLVPECL}	LVPECL	0.23	0.38	0.38	0.38	ns, max
	T _{GPCCI33_3}	PCI, 33 MHz, 3.3 V	-0.05	0.08	0.08	0.08	ns, max
	T _{GPCCI66_3}	PCI, 66 MHz, 3.3 V	-0.05	-0.11	-0.11	-0.11	ns, max
	T _{GPGTL}	GTL	0.20	0.37	0.37	0.37	ns, max
	T _{GPGTLP}	GTL+	0.20	0.37	0.37	0.37	ns, max
	T _{GPHSTL}	HSTL	0.18	0.27	0.27	0.27	ns, max
	T _{GPSSTL2}	SSTL2	0.21	0.27	0.27	0.27	ns, max
	T _{GPSSTL3}	SSTL3	0.18	0.27	0.27	0.27	ns, max
	T _{GPCTT}	CTT	0.22	0.33	0.33	0.33	ns, max
T _{GPAGP}	AGP	0.21	0.27	0.27	0.27	ns, max	

Notes:

- Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 2](#).
- The numbers for Min are **Advance** product specification numbers.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see [Figure 2](#). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description ¹	Symbol	Speed Grade				Units
		Min ²	-8	-7	-6	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.34	0.87	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.40	0.87	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T_{ICK} / T_{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK} / T_{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK} / T_{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK} / T_{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK} / T_{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK} / T_{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK} / T_{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	-	416	400	357.2	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

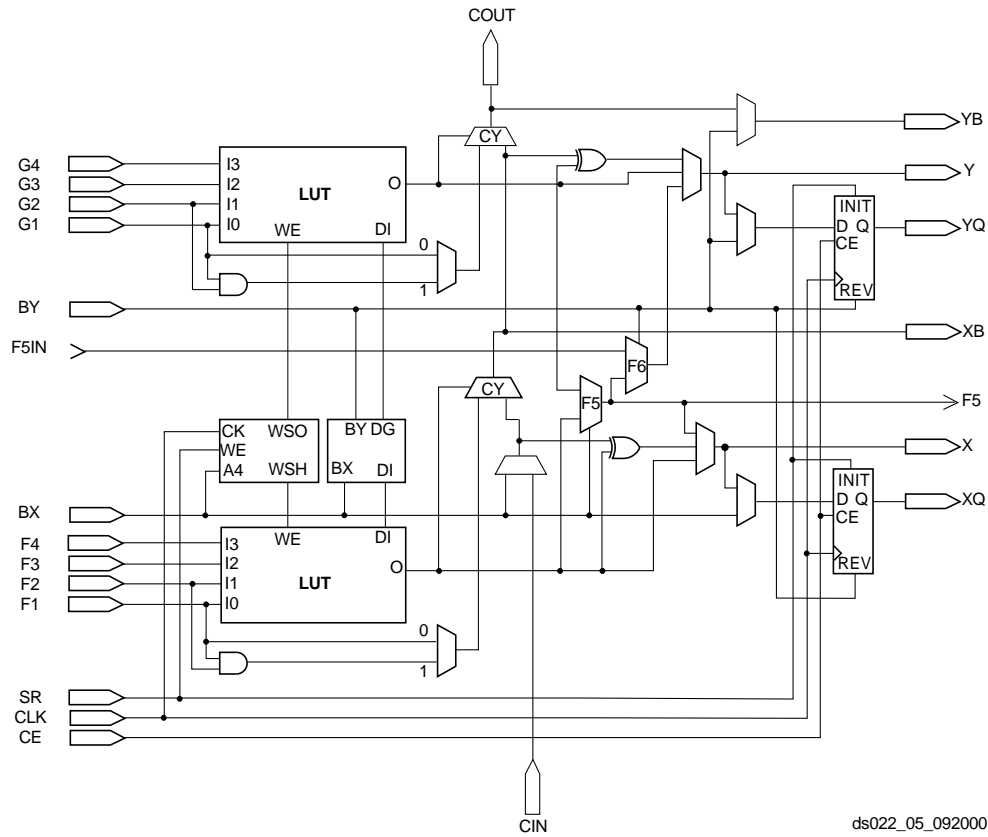


Figure 2: Detailed View of Virtex-E Slice

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CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description ¹	Symbol	Speed Grade				Units
		Min ²	-8	-7	-6	
Combinatorial Delays						
F operand inputs to X via XOR	T _{OPX}	0.32	0.68	0.8	0.8	ns, max
F operand input to XB output	T _{OPXB}	0.35	0.65	0.8	0.9	ns, max
F operand input to Y via XOR	T _{OPY}	0.59	1.06	1.4	1.5	ns, max
F operand input to YB output	T _{OPYB}	0.48	0.89	1.1	1.3	ns, max
F operand input to COUT output	T _{OPCYF}	0.37	0.71	0.9	1.0	ns, max
G operand inputs to Y via XOR	T _{OPGY}	0.34	0.72	0.8	0.9	ns, max
G operand input to YB output	T _{OPGYB}	0.47	0.78	1.2	1.3	ns, max
G operand input to COUT output	T _{OPCYG}	0.36	0.60	0.9	1.0	ns, max
BX initialization input to COUT	T _{BXCY}	0.19	0.36	0.51	0.57	ns, max
CIN input to X output via XOR	T _{CINX}	0.27	0.50	0.6	0.7	ns, max
CIN input to XB	T _{CINXB}	0.02	0.03	0.07	0.08	ns, max
CIN input to Y via XOR	T _{CINY}	0.26	0.45	0.7	0.7	ns, max
CIN input to YB	T _{CINYB}	0.16	0.28	0.38	0.43	ns, max
CIN input to COUT output	T _{BYP}	0.05	0.10	0.14	0.15	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T _{FANDXB}	0.10	0.30	0.35	0.39	ns, max
F1/2 operand inputs to YB output via AND	T _{FANDYB}	0.28	0.56	0.7	0.8	ns, max
F1/2 operand inputs to COUT output via AND	T _{FANDCY}	0.17	0.38	0.46	0.51	ns, max
G1/2 operand inputs to YB output via AND	T _{GANDYB}	0.20	0.46	0.55	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T _{GANDCY}	0.09	0.28	0.30	0.34	ns, max
Setup and Hold Times before/after Clock CLK						
CIN input to FFX	T _{CCKX} /T _{CKCX}	0.47 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T _{CCKY} /T _{CKCY}	0.49 / 0	0.92 / 0	1.2 / 0	1.3 / 0	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

CLB Distributed RAM Switching Characteristics

Description ¹	Symbol	Speed Grade				Units
		Min ²	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.48	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.76	1.9	2.1	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T_{REG}	1.25	2.49	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.24 / 0	0.47 / 0	0.53 / 0	0.6 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T_{SHDICK}	0.24 / 0	0.47 / 0	0.53 / 0	0.6 / 0	ns, min
CE input (WS)	$T_{SHCHECK}$	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

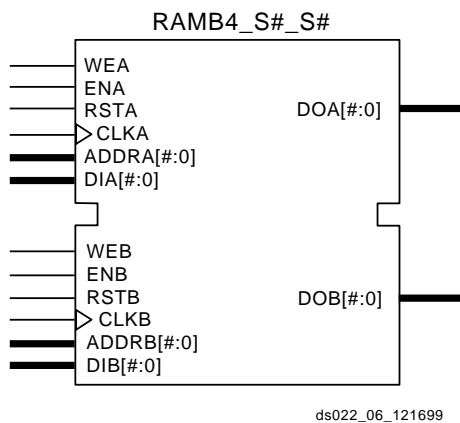


Figure 3: Dual-Port Block SelectRAM

Block RAM Switching Characteristics

Description ¹	Symbol	Speed Grade				Units
		Min ²	-8	-7	-6	
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The numbers for Min are **Advance** product specification numbers.

TBUF Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min ¹	-8	-7	-6	
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0.0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

Notes:

1. The numbers for Min are **Advance** product specification numbers.

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Virtex-E Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description ¹	Symbol	Device ³	Speed Grade ²				Units
			Min ⁴	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust the delays with the values shown in “IOB Output Switching Characteristics Standard Adjustments” on page 8.	T _{ICKOFDLL}	XCV405E	1.0	3.1	3.1	3.1	ns
		XCV812E	1.0	3.1	3.1	3.1	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 1](#) and [Table 2](#).
3. DLL output jitter is already included in the timing calculation.
4. The numbers for Min are **Advance** product specification numbers.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description ¹	Symbol	Device	Speed Grade ²				Units
			Min ³	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust the delays with the values shown in “IOB Output Switching Characteristics Standard Adjustments” on page 8.	T _{ICKOF}	XCV405E	1.6	4.5	4.7	4.9	ns
		XCV812E	1.8	4.8	5.0	5.2	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 1](#) and [Table 2](#).
3. The numbers for Min are **Advance** product specification numbers.

Virtex-E Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Set-Up and Hold for LVTTTL Standard, *with* DLL

Description ¹	Symbol	Device ³	Speed Grade ²				Units
			Min ⁴	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in “IOB Input Switching Characteristics Standard Adjustments” on page 6.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV405E	1.5 / -0.4	1.5 / -0.4	1.6 / -0.4	1.7 / -0.4	ns
Global Clock and IFF, with DLL		XCV812E	1.5 / -0.4	1.5 / -0.4	1.6 / -0.4	1.7 / -0.4	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. The numbers for Min are **Advance** product specification numbers.

Global Clock Set-Up and Hold for LVTTTL Standard, *without* DLL

Description ¹	Symbol	Device ³	Speed Grade ²				Units
			Min ⁴	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in “IOB Input Switching Characteristics Standard Adjustments” on page 6.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV405E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV812E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
4. The numbers for Min are **Advance** product specification numbers.

DLL Timing Parameters

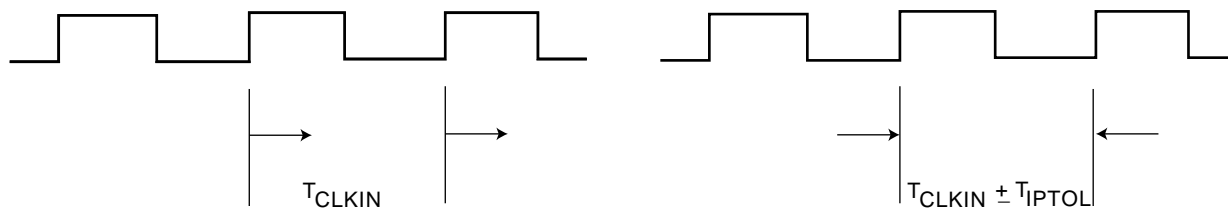
Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade ¹						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	320	60	320	60	260	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥ 25 MHz	5.0		5.0		5.0		ns
		≥ 50 MHz	3.0		3.0		3.0		ns
		≥ 100 MHz	2.4		2.4		2.4		ns
		≥ 150 MHz	2.0		2.0		2.0		ns
		≥ 200 MHz	1.8		1.8		1.8		ns
		≥ 250 MHz	1.5		1.5		1.5		ns
		≥ 300 MHz	1.3		1.3		NA		ns

Notes:

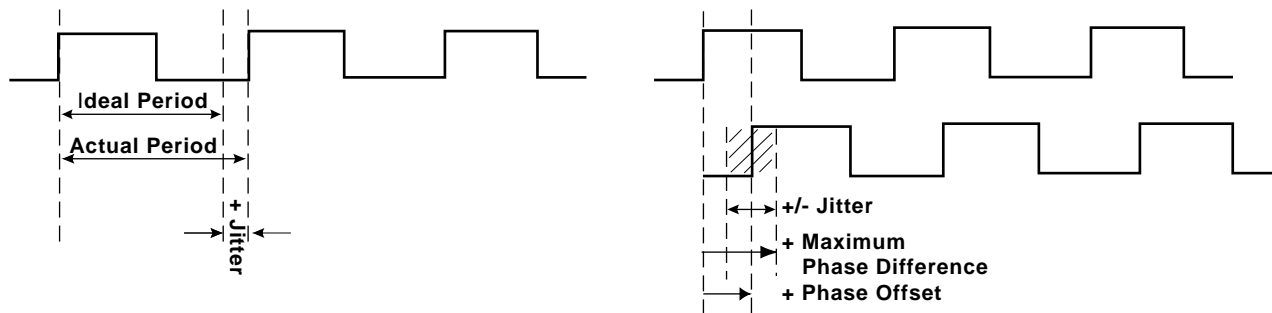
- All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference



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Figure 4: DLL Timing Waveforms

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Description	Symbol	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output ¹	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO ²	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL ³	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO ⁴	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL ⁵	T_{PHOOM}			± 200		± 200	ps

Notes:

- Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
- Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
- Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
- Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
- Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
- All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/00	1.0	Initial Xilinx release.
08/01/00	1.1	Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table.
09/19/00	1.2	<ul style="list-style-type: none"> In Table 3 (Module 4), FG676 Fine-Pitch BGA — XCV405E, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1. Min values added to Virtex-E Electrical Characteristics tables.
11/20/00	1.3	<ul style="list-style-type: none"> Updated speed grade -8 numbers in Virtex-E Electrical Characteristics tables (Module 3). Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). Added to note 2 of Absolute Maximum Ratings (Module 3). Changed all minimum hold times to -0.4 for Global Clock Set-Up and Hold for LVTTL Standard, with DLL (Module 3). Revised maximum T_{DLLPW} in -6 speed grade for DLL Timing Parameters (Module 3).
04/02/01	1.4	<ul style="list-style-type: none"> In Table 4, FG676 Fine-Pitch BGA — XCV405E, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. Updated values in Virtex-E Switching Characteristics tables. Converted data sheet to modularized format. See the Virtex-E Extended Memory Data Sheet section.
04/19/01	1.5	<ul style="list-style-type: none"> Updated values in Virtex-E Switching Characteristics tables.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: [Introduction and Ordering Information \(Module 1\)](#)
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: [Functional Description \(Module 2\)](#)
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: [Pinout Tables \(Module 4\)](#)