Virtex™-II Electrical Characteristics

Virtex-II devices are provided in -4, -5, and -6 speed grades, with -6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -4 speed grade industrial device are the same as for a -4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal Supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.0	V
V_{REF}	Input Reference Voltage	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5 to 4.0	V
V_{CCINT}	Longest Supply Voltage Rise Time from 0 V - 1.425 V	50	ms
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temp.	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Power supplies might turn on in any order.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	3.0	3.6	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If V_{CCAUX} and V_{CCO} are both at 3.3 V, they must use a common supply voltage.
2. If battery is not used, do not connect V_{BATT}.
3. For LVDS operation, V_{CCAUX} min is 3.13 V and max is 3.47 V.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)	All	1.2		V
V_{DRI}	Data Retention V_{CCAUX} Voltage (below which configuration data might be lost)	All	2.5		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current[1]	Device Dependent			
I_{CCOQ}	Quiescent V_{CCO} supply current[1]	Device Dependent			
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current[1]	Device Dependent			
I_{REF}	V_{REF} current per bank	All			µA
I_L	Input or output leakage current	All			µA
C_{IN}	Input capacitance (sample tested)	All			pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note 2		mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)	All	Note 2		mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Data are retained even if V_{CCO} drops to 0 V.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms).

Table 4: **Supply Current Requirements**

Product	Description[2]	Current Requirement[3]
Virtex-II Family, Commercial Grade	Minimum required current supply	500 mA
Virtex-II Family, Industrial Grade	Minimum required current supply	500 mA

Notes:
1. Ramp rate used for this specification is from 0 to 1.5 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents may result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 5: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	V_{CCO} – 0.45	16	– 16
LVCMOS15	– 0.5	20% V_{CCO}	70% V_{CCO}	1.65	0.4	V_{CCO} – 0.45	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	1.5	0.4	V_{CCO} – 0.4	48	– 8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	2.7	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	2.7	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP–2X	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.

LDT DC Specifications (LDT_25)

Table 6: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	530	600	740	mV
Change in V_{OD} Magnitude	ΔV_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals			30	mV
Output Common Mode Voltage	V_{OS}	R_T = 100 ohm across Q and $\overline{Q}$ signals	550	600	680	mV
Change in V_{OS} Magnitude	ΔV_{OS}				30	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 7: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.475	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 8: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.70	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V				mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV				V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 9 summarizes the DC output specifications of LVPECL.

Table 9: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as **Virtex-II Switching Characteristics**, page 7 (speed files).

Table 10 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 10: **Pin-to-Pin Performance**

Description	Pin-to-Pin (w/ I/O delays)	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	6.7	XC2V1000 -5
32-bit Address Decoder	8.0	XC2V1000 -5
64-bit Address Decoder	9.6	XC2V1000 -5
4:1 MUX	6.0	XC2V1000 -5
8:1 MUX	6.8	XC2V1000 -5
16:1 MUX	6.8	XC2V1000 -5
32:1 MUX	8.9	XC2V1000 -5
Combinatorial (pad to LUT to pad)	5.4	XC2V1000 -5
Memory		
Block RAM		
Pad to setup	N/A	
Clock to Pad	N/A	
Distributed RAM		
Pad to setup	2.9	XC2V1000 -5
Clock to Pad	5.3 (no clk skew)	XC2V1000 -5

Table 11 shows internal (register-to-register) performance. Values are reported in MHz.

Table 11: **Register-to-Register Performance**

Description	Register-to-Register Performance	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	460	XC2V1000 -5
32-bit Address Decoder	312.5	XC2V1000 -5
64-bit Address Decoder	264.6	XC2V1000 -5
4:1 MUX	554	XC2V1000 -5
8:1 MUX	516.5	XC2V1000 -5
16:1 MUX	428	XC2V1000 -5
32:1 MUX	371.2	XC2V1000 -5
Register to LUT to Register	715.3	XC2V1000 -5
8-bit Adder	315.2	XC2V1000 -5
16-bit Adder	284.8	XC2V1000 -5
64-bit Adder	171.2	XC2V1000 -5
64-bit Counter	186.2	XC2V1000 -5
64-bit Accumulator	116.9	XC2V1000 -5
Multiplier 18x18 (with Block RAM inputs)	103.8	XC2V1000 -5
Multiplier 18x18 (with Register inputs)	147.3	XC2V1000 -5
Memory		
Block RAM		
Single-Port 4096 x 4 bits	N/A	
Single-Port 2048 x 9 bits	N/A	
Single-Port 1024 x 18 bits	N/A	
Single-Port 512 x 36 bits	N/A	
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits	N/A	
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits	N/A	
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits	N/A	
Distributed RAM		
Single-Port 32 x 8-bit	481.0	XC2V1000 -5
Single-Port 64 x 8-bit	405.8	XC2V1000 -5
Single-Port 128 x 8-bit	343.4	XC2V1000 -5
Dual-Port 16 x 8	264.9	XC2V1000 -5
Dual-Port 32 x 8	414.3	XC2V1000 -5
Dual-Port 64 x 8	363.4	XC2V1000 -5
Dual-Port 128 x 8	318.7	XC2V1000 -5
Shift Registers		
128-bit SRL	N/A	
256-bit SRL	N/A	

Table 11: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Device Used & Speed Grade
FIFOs (Async. in Block RAM)		
1024 x 18-bit	N/A	
1024 x 18-bit	N/A	
FIFOs (Sync. in SRL)		
128 x 8-bit	N/A	
128 x 16-bit	N/A	
CAMs in Block RAM		
32 x 9-bit	N/A	
64 x 9-bit	N/A	
128 x 9-bit	N/A	
256 x 9-bit	N/A	
CAMs in SRL		
32 x 16-bit	N/A	
64 x 32-bit	N/A	
128 x 40-bit	N/A	
256 x 48-bit	N/A	
1024 x 16-bit	N/A	
1024 x 72-bit	N/A	

Virtex-II Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Final. Note that **Virtex-II Performance Characteristics**, page 5 are subject to these guidelines, as well. The status of each designation is defined as follows:

Advance:These speed files are based on additional simulation and testing of some family members. Although speed grades with this designation are considered relatively stable, some under-reporting might still occur. All family members do not necessarily transition to “Advance” at the same time. Typically, the slowest speed grades transition to “Advance” before faster speed grades.

Preliminary:Preliminary speed files are based on full device characterization. Devices and speed grades with this designation are considered safe for use in production designs. There are no under-reported delays.

Final:Final speed files are released once the family has enough production history and full correlation between the speeds files and devices is established over numerous production lots.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.

Table 12: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All		0.61	0.70	ns, max
Pad to I output, with delay	T_{IOPID}			2.61	3.00	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All		0.82	0.94	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}			2.82	3.24	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.66	0.76	ns, max
Setup and Hold Times With Respect to Clock at IOB **Input Register**						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All		0.69 / 0.00	0.79 / 0.00	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$			2.69 / 0.00	3.09 / 0.00	ns, min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21 / 0.00	0.24 / 0.00	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All		0.19	0.21	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All		0.32	0.36	ns, max
GSR to output IQ	T_{GSRQ}	All		7.66	8.81	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 17.

IOB Input Switching Characteristics Standard Adjustments

Table 13: **IOB Input Switching Characteristics Standard Adjustments**

Description	Symbol	Standard	Speed Grade			Units
			–6	–5	–4	
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL		0.00	0.00	ns
	$T_{ILVCMOS33}$	LVCMOS33		0.00	0.00	ns
	$T_{ILVCMOS25}$	LVCMOS25		0.11	0.12	ns
	$T_{ILVCMOS18}$	LVCMOS18		0.43	0.49	ns
	$T_{ILVCMOS15}$	LVCMOS15		1.00	1.14	ns
	T_{ILVDS_25}	LVDS_25		0.60	0.69	ns
	T_{ILVDS_33}	LVDS_33		0.60	0.69	ns
	$T_{ILVPECL\_33}$	LVPECL		0.60	0.69	ns

Table 13: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V		0.00	0.00	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V		0.00	0.00	ns
	T_{IPCIX}	PCI–X, 133 MHz, 3.3 V		0.00	0.00	ns
	T_{IGTL}	GTL		0.42	0.48	ns
	$T_{IGTLPLUS}$	GTLP		0.42	0.48	ns
	T_{IHSTL_I}	HSTL I		0.42	0.48	ns
	T_{IHSTL_II}	HSTL II		0.42	0.48	ns
	T_{IHSTL_III}	HSTL III		0.42	0.48	ns
	T_{IHSTL_IV}	HSTL IV		0.42	0.48	ns
	T_{ISSTL2_I}	SSTL2 I		0.42	0.48	ns
	T_{ISSTL2_II}	SSTL2 II		0.42	0.48	ns
	T_{ISSTL3_I}	SSTL3 I		0.35	0.40	ns
	T_{ISSTL3_II}	SSTL3 II		0.35	0.40	ns
	T_{IAGP}	AGP–2X		0.35	0.40	ns
	$T_{ILVDCI33}$	LVDCI_33		0.00	0.00	ns
	$T_{ILVDCI25}$	LVDCI_25		0.11	0.12	ns
	$T_{ILVDCI18}$	LVDCI_18		0.43	0.49	ns
	$T_{ILVDCI15}$	LVDCI_15		1.00	1.14	ns
	$T_{ILVDCI\_DV2\_33}$	LVDCI_DV2_33		0.00	0.00	ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25		0.11	0.12	ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18		0.43	0.49	ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15		1.00	1.14	ns
	T_{IGTL_DCI}	GTL_DCI		0.42	0.48	ns
	T_{IGTLP_DCI}	GTLP_DCI		0.42	0.48	ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI		0.42	0.48	ns
	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI		0.42	0.48	ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI		0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI		0.42	0.48	ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI		0.42	0.48	ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI		0.42	0.48	ns
	$T_{ISSTL3\_I\_DCI}$	SSTL3_I_DCI		0.35	0.40	ns
	$T_{ISSTL3\_II\_DCI}$	SSTL3_II_DCI		0.35	0.40	ns
	T_{ILDT_25}	LDT_25		0.49	0.56	ns
	T_{IULVDS_25}	ULVDS_25		0.49	0.56	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 17.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.

Table 14: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–6**	**–5**	**–4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}		2.88	3.31	ns, max
O input to Pad via transparent latch	T_{IOOLP}		3.09	3.55	ns, max
3-State Delays					
T input to Pad high-impedance (Note 2)	T_{IOTHZ}		2.37	2.73	ns, max
T input to valid data on Pad	T_{IOTON}		2.37	2.73	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$		2.58	2.97	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		2.58	2.97	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}		6.89	7.92	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}		3.24	3.73	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}		2.88	3.32	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		2.88	3.32	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}		0.19/0.00	0.21/0.00	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$		0.21/0.00	0.24/0.00	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$		0.19/0.00	0.21/0.00	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}		0.22/0.00	0.26/0.00	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$		0.21/0.00	0.24/0.00	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$		0.19/0.00	0.21/0.00	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}		3.08	3.55	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}		2.54	2.92	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		2.54	2.92	ns, max
GSR to Pad	T_{IOGSRQ}		5.98	6.88	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 15: **IOB Output Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA		11.13	12.80	ns
	T_{OLVTTL_S4}	4 mA		6.87	7.90	ns
	T_{OLVTTL_S6}	6 mA		4.79	5.50	ns
	T_{OLVTTL_S8}	8 mA		3.40	3.91	ns
	T_{OLVTTL_S12}	12 mA		2.61	3.00	ns
	T_{OLVTTL_S16}	16 mA		1.83	2.10	ns
	T_{OLVTTL_S24}	24 mA		1.22	1.40	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA		7.66	8.80	ns
	T_{OLVTTL_F4}	4 mA		3.05	3.50	ns
	T_{OLVTTL_F6}	6 mA		1.83	2.10	ns
	T_{OLVTTL_F8}	8 mA		0.27	0.30	ns
	T_{OLVTTL_F12}	12 mA		0.00	0.00	ns
	T_{OLVTTL_F16}	16 mA		–0.44	–0.50	ns
	T_{OLVTTL_F24}	24 mA		–0.52	–0.60	ns
	T_{OLVDS_25}	LVDS		–1.12	–1.29	ns
	T_{OLVDS_33}	LVDS		–1.18	–1.36	ns
	$T_{OLVDSEXT\_25}$	LVDS		–1.03	–1.19	ns
	$T_{OLVDSEXT\_33}$	LVDS		–1.05	–1.21	ns
	T_{OLDT_25}	LDT		–1.11	–1.28	ns
	T_{OBLVDS_25}	BLVDS				ns
	T_{OULVDS_25}	ULVDS		–1.11	–1.28	ns
	$T_{OLVPECL\_33}$	LVPECL		0.81	0.93	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V		2.79	3.20	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V		0.27	0.30	ns
	T_{OPCIX}	PCI–X, 133 MHz, 3.3 V		0.27	0.30	ns
	T_{OGTL}	GTL		0.00	0.00	ns
	T_{OGTLP}	GTLP		0.00	0.00	ns
	T_{OHSTL_I}	HSTL I		0.18	0.20	ns
	T_{OHSTL_II}	HSTL II		–0.17	–0.20	ns
	T_{OHSTL_IIII}	HSTL III		–0.34	–0.40	ns
	T_{OHSTL_IV}	HSTL IV		–0.52	–0.60	ns
	T_{OSSTL2_I}	SSTL2 I		–0.09	–0.10	ns
	T_{OSSTL2_II}	SSTL2 II		–0.34	–0.40	ns

Table 15: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{OSSTL3_I}	SSTL3 I		0.00	0.00	ns
	T_{OSSTL3_II}	SSTL3 II		–0.17	–0.20	ns
	T_{OAGP}	AGP–2X		–0.26	–0.30	ns
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA		9.66	11.10	ns
	$T_{OLVCMOS33\_S4}$	4 mA		5.51	6.33	ns
	$T_{OLVCMOS33\_S6}$	6 mA		4.00	4.60	ns
	$T_{OLVCMOS33\_S8}$	8 mA		2.70	3.10	ns
	$T_{OLVCMOS33\_S12}$	12 mA		2.27	2.60	ns
	$T_{OLVCMOS33\_S16}$	16 mA		1.40	1.60	ns
	$T_{OLVCMOS33\_S24}$	24 mA		1.31	1.50	ns
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA		7.22	8.30	ns
	$T_{OLVCMOS33\_F4}$	4 mA		3.13	3.60	ns
	$T_{OLVCMOS33\_F6}$	6 mA		1.40	1.60	ns
	$T_{OLVCMOS33\_F8}$	8 mA		0.27	0.30	ns
	$T_{OLVCMOS33\_F12}$	12 mA		0.00	0.00	ns
	$T_{OLVCMOS33\_F16}$	16 mA		–0.34	–0.40	ns
	$T_{OLVCMOS33\_F24}$	24 mA		–0.52	–0.60	ns
	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA		11.22	12.90	ns
	$T_{OLVCMOS25\_S4}$	4 mA		6.44	7.40	ns
	$T_{OLVCMOS25\_S6}$	6 mA		5.83	6.70	ns
	$T_{OLVCMOS25\_S8}$	8 mA		5.05	5.80	ns
	$T_{OLVCMOS25\_S12}$	12 mA		3.66	4.20	ns
	$T_{OLVCMOS25\_S16}$	16 mA		2.96	3.40	ns
	$T_{OLVCMOS25\_S24}$	24 mA		2.61	3.00	ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA		5.57	6.40	ns
	$T_{OLVCMOS25\_F4}$	4 mA		1.74	2.00	ns
	$T_{OLVCMOS25\_F6}$	6 mA		1.05	1.20	ns
	$T_{OLVCMOS25\_F8}$	8 mA		0.70	0.80	ns
	$T_{OLVCMOS25\_F12}$	12 mA		0.18	0.20	ns
	$T_{OLVCMOS25\_F16}$	16 mA		0.00	0.00	ns
	$T_{OLVCMOS25\_F24}$	24 mA		–0.17	–0.20	ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA		20.18	23.20	ns
	$T_{OLVCMOS18\_S4}$	4 mA		13.74	15.80	ns
	$T_{OLVCMOS18\_S6}$	6 mA		10.35	11.90	ns
	$T_{OLVCMOS18\_S8}$	8 mA		9.57	11.00	ns
	$T_{OLVCMOS18\_S12}$	12 mA		8.18	9.40	ns
	$T_{OLVCMOS18\_S16}$	16 mA		7.74	8.90	ns

Table 15: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA		7.66	8.80	ns
	$T_{OLVCMOS18\_F4}$	4 mA		3.48	4.00	ns
	$T_{OLVCMOS18\_F6}$	6 mA		1.57	1.80	ns
	$T_{OLVCMOS18\_F8}$	8 mA		1.40	1.60	ns
	$T_{OLVCMOS18\_F12}$	12 mA		0.70	0.80	ns
	$T_{OLVCMOS18\_F16}$	16 mA		0.61	0.70	ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA		25.57	29.40	ns
	$T_{OLVCMOS15\_S4}$	4 mA		18.09	20.80	ns
	$T_{OLVCMOS15\_S6}$	6 mA		16.79	19.30	ns
	$T_{OLVCMOS15\_S8}$	8 mA		14.53	16.70	ns
	$T_{OLVCMOS15\_S12}$	12 mA		13.31	15.30	ns
	$T_{OLVCMOS15\_S16}$	16 mA		12.53	14.40	ns
	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA		7.48	8.60	ns
	$T_{OLVCMOS15\_F4}$	4 mA		3.83	4.40	ns
	$T_{OLVCMOS15\_F6}$	6 mA		2.79	3.20	ns
	$T_{OLVCMOS15\_F8}$	8 mA		1.74	2.00	ns
	$T_{OLVCMOS15\_F12}$	12 mA		1.40	1.60	ns
	$T_{OLVCMOS15\_F16}$	16 mA		1.40	1.60	ns
	$T_{OLVDCI33}$	LVDCI_33		0.09	0.10	ns
	$T_{OLVDCI25}$	LVDCI_25		0.18	0.20	ns
	$T_{OLVDCI18}$	LVDCI_18		0.44	0.50	ns
	$T_{OLVDCI15}$	LVDCI_15		0.53	0.60	ns
	$T_{OLVDCI\_DV2\_33}$	LVDCI_DV2_33		–0.87	–1.00	ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25		–0.69	–0.80	ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18		–0.60	–0.70	ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15		–0.43	–0.50	ns
	T_{OGTL_DCI}	GTL_DCI		0.35	0.40	ns
	T_{OGTLP_DCI}	GTLP_DCI		0.27	0.30	ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI		0.18	0.20	ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI		–0.17	–0.20	ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI		–0.34	–0.40	ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI		–0.52	–0.60	ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI		–0.09	–0.10	ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI		–0.34	–0.40	ns
	$T_{OSSTL3\_I\_DCI}$	SSTL3_I_DCI		0.00	0.00	ns
	$T_{OSSTL3\_II\_DCI}$	SSTL3_II_DCI		–0.17	–0.20	ns

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard, as listed in Table 16.

Table 16: **Constants for Use in Calculation of T_{IOOP}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	
LVTTL Fast Slew Rate, 4mA drive	35	
LVTTL Fast Slew Rate, 6mA drive	35	
LVTTL Fast Slew Rate, 8mA drive	35	
LVTTL Fast Slew Rate, 12mA drive	35	
LVTTL Fast Slew Rate, 16mA drive	35	
LVTTL Fast Slew Rate, 24mA drive	35	
LVTTL Slow Slew Rate, 2mA drive	35	
LVTTL Slow Slew Rate, 4mA drive	35	
LVTTL Slow Slew Rate, 6mA drive	35	
LVTTL Slow Slew Rate, 8mA drive	35	
LVTTL Slow Slew Rate, 12mA drive	35	
LVTTL Slow Slew Rate, 16mA drive	35	
LVTTL Slow Slew Rate, 24mA drive	35	
LVCMOS33	35	
LVCMOS25	35	
LVCMOS18	35	
LVCMOS15	35	
PCI 33MHZ 3.3 V	10	
PCI 66 MHz 3.3 V	10	
PCI–X 133 MHz 3.3 V	10	
GTL	0	
GTLP	0	
HSTL Class I	20	
HSTL Class II	20	
HSTL Class III	20	
HSTL Class IV	20	
SSTL2 Class I	30	
SSTL2 Class II	30	
SSTL3 Class I	30	
SSTL3 Class II	30	
AGP–2X	10	

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{IOOP}.

$$T_{IOOP} = T_{IOOP} + T_{OPADJUST} + (C_{LOAD} - C_{SL}) * fl$$

Where:

$T_{OPADJUST}$ is reported above in the Output Delay Adjustment section.

C_{LOAD} is the capacitive load for the design.

Table 17: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
PCIX33_3	Per PCI–X Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
AGP–2X	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in Table 16.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
5. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Table 18: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
GCLK IOB **and Buffer**					
Global Clock PAD to output.	T_{GPIO}		0.36	0.41	ns, max
Global Clock Buffer I input to O output	T_{GIO}		0.23	0.26	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 14). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 19: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}		0.39	0.45	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}		0.58	0.67	ns, max
5-input function: F/G inputs to X output	T_{IF5X}		0.77	0.88	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}		0.33	0.38	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}		0.25	0.28	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}		0.25	0.28	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}		0.49	0.56	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}		0.33	0.37	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}		0.42	0.48	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}		0.61	0.70	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}		0.28/0.00	0.32/0.00	ns, min
DY inputs	T_{DYCK}/T_{CKDY}		0.19/0.00	0.22/0.00	ns, min
DX inputs	T_{DXCK}/T_{CKDX}		0.19/0.00	0.22/0.00	ns, min
CE input	T_{CECK}/T_{CKCE}		0.21/0.00	0.24/0.00	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}		0.19/ 0.00	0.22/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}		0.57	0.66	ns, min
Minimum Pulse Width, Low	T_{CL}		0.57	0.66	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}		0.57	0.66	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}		0.25	0.29	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}		880	765	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Table 20: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$		1.78	2.04	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$		2.09	2.41	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$		1.89	2.17	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		0.67/0.00	0.77/0.00	ns, min
F/G address inputs	T_{AS}/T_{AH}		0.44/0.00	0.50/0.00	ns, min
CE input (WE)	T_{WES}/T_{WEH}		0.46/0.00	0.53/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}		0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{WPL}		0.63	0.72	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		1.25	1.44	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 21: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}		2.53	2.91	ns, max
Clock CLK to X/Y outputs	T_{REG32}		2.84	3.27	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}		2.45	2.82	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}		2.39	2.75	ns, max
Clock CLK to Shiftout	T_{CKSH}		2.17	2.49	ns, max
Clock CLK to F5 output	T_{REGF5}		2.64	3.04	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}		0.28/0.00	0.32/0.00	ns, min
CE input (WS)	T_{WSS}/T_{WSH}		0.21/0.00	0.24/0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}		0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{SRPL}		0.63	0.72	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Multiplier Switching Characteristics

Table 22: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT}		4.34	4.98	ns, max
Input to Pin34	T_{MULT}		4.22	4.85	ns, max
Input to Pin33	T_{MULT}		4.11	4.72	ns, max
Input to Pin32	T_{MULT}		3.99	4.59	ns, max
Input to Pin31	T_{MULT}		3.88	4.46	ns, max
Input to Pin30	T_{MULT}		3.77	4.33	ns, max
Input to Pin29	T_{MULT}		3.65	4.20	ns, max
Input to Pin28	T_{MULT}		3.54	4.07	ns, max
Input to Pin27	T_{MULT}		3.42	3.93	ns, max
Input to Pin26	T_{MULT}		3.31	3.80	ns, max
Input to Pin25	T_{MULT}		3.20	3.67	ns, max
Input to Pin24	T_{MULT}		3.08	3.54	ns, max
Input to Pin23	T_{MULT}		2.97	3.41	ns, max
Input to Pin22	T_{MULT}		2.85	3.28	ns, max
Input to Pin21	T_{MULT}		2.74	3.15	ns, max
Input to Pin20	T_{MULT}		2.63	3.02	ns, max
Input to Pin19	T_{MULT}		2.51	2.89	ns, max
Input to Pin18	T_{MULT}		2.40	2.76	ns, max
Input to Pin17	T_{MULT}		2.28	2.62	ns, max
Input to Pin16	T_{MULT}		2.17	2.49	ns, max
Input to Pin15	T_{MULT}		2.06	2.36	ns, max
Input to Pin14	T_{MULT}		1.94	2.23	ns, max
Input to Pin13	T_{MULT}		1.83	2.10	ns, max
Input to Pin12	T_{MULT}		1.71	1.97	ns, max
Input to Pin11	T_{MULT}		1.60	1.84	ns, max
Input to Pin10	T_{MULT}		1.49	1.71	ns, max
Input to Pin9	T_{MULT}		1.37	1.58	ns, max
Input to Pin8	T_{MULT}		1.26	1.45	ns, max
Input to Pin7	T_{MULT}		1.14	1.31	ns, max
Input to Pin6	T_{MULT}		1.03	1.18	ns, max
Input to Pin5	T_{MULT}		0.92	1.05	ns, max
Input to Pin4	T_{MULT}		0.80	0.92	ns, max
Input to Pin3	T_{MULT}		0.69	0.79	ns, max
Input to Pin2	T_{MULT}		0.57	0.66	ns, max
Input to Pin1	T_{MULT}		0.46	0.53	ns, max
Input to Pin0	T_{MULT}		0.35	0.40	ns, max

Block SelectRAM Switching Characteristics

Table 23: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}		3.01	3.46	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}		0.32/ 0.00	0.36/ 0.00	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}		0.32/ 0.00	0.36/ 0.00	ns, min
EN input	T_{BECK}/T_{BCKE}		1.04/ 0.00	1.20/ 0.00	ns, min
RST input	T_{BRCK}/T_{BCKR}		1.44/ 0.00	1.65/ 0.00	ns, min
WEN input	T_{BWCK}/T_{BCKW}		0.63/ 0.30	0.72/ 0.00	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}		1.51	1.74	ns, min
Minimum Pulse Width, Low	T_{BPWL}		1.51	1.74	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 24: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
IN input to OUT output	T_{IO}		0.25	0.29	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.48	0.55	ns, max
TRI input to valid data on OUT output	T_{ON}		0.48	0.55	ns, max

JTAG Test Access Port Switching Characteristics

Table 25: **JTAG Test Access Port Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
TMS and TDI Setup times before TCK	T_{TAPTK}				ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}				ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}				ns, max
Maximum TCK clock frequency	F_{TCK}				MHz, max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 26: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.	$T_{ICKOFDCM}$					ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 16 and Table 17.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 27: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 11.	T_{ICKOF}	2V1000		5.20	5.98	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 16 and Table 17.
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *With* DCM

Table 28: **Global Clock Set-Up and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.						
No Delay Global Clock and IFF	T_{PSDCM}/T_{PHDCM}					ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *Without* DCM

Table 29: **Global Clock Set-Up and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.						
Full Delay Global Clock and IFF	T_{PSFD}/T_{PHFD}	2V1000		1.8/0.0	2.1/0.0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DCM Timing Parameters

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605; all devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 30: **Operating Frequency Ranges**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Output Clocks (Low Frequency Mode)									
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF				24	210	24	180	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF				48	420	48	360	MHz
CLKDV	CLKOUT_FREQ_DV_LF				1.5	140	1.5	120	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF				24	240	24	200	MHz
Input Clocks (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_FREQ_DLL_LF				24	210	24	180	MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_LF				12	240	12	200	MHz
PSCLK	PSCLK_FREQ_LF				0.01	210	0.01	180	MHz
Output Clocks (High Frequency Mode)									
CLK0, CLK180	CLKOUT_FREQ_1X_HF				48	420	48	360	MHz
CLKDV	CLKOUT_FREQ_DV_HF				3	280	3	240	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF				160	320	160	270	MHz
Input Clocks (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_FREQ_DLL_HF				48	420	48	360	MHz
CLKIN (using CLKFX outputs)	CLKIN_FREQ_FX_HF				32	320	32	270	MHz
PSCLK	PSCLK_FREQ_HF				0.01	420	0.01	365	MHz

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Input Clock Tolerances

Table 31: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz			25.00		25.00		ns
CLKIN[2]	CLKIN_PULSE	1 - 10 MHz			25.00		25.00		ns
		10 - 25 MHz			10.00		10.00		ns
		25 - 50 MHz			5.00		5.00		ns
		50 - 100 MHz			3.00		3.00		ns
		100 - 150 MHz			2.40		2.40		ns
		150 - 200 MHz			2.00		2.00		ns
		200 - 250 MHz			1.80		1.80		ns
		250 - 300 MHz			1.50		1.50		ns
		300 - 350 MHz			1.30		1.30		ns
		350 - 400 MHz			1.15		1.15		ns
		> 400 MHz			1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_CYC_JITT_DLL_LF					±300		±300	ps
CLKIN (using CLKFX outputs)	CLKIN_CYC_JITT_FX_LF					±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_CYC_JITT_DLL_HF					±150		±150	ps
CLKIN (using CLKFX outputs)	CLKIN_CYC_JITT_FX_HF					±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_PER_JITT_DLL_LF					±1.00		±1.00	ns
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_LF					±1.00		±1.00	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs[1])	CLKIN_PER_JITT_DLL_HF					±1.00		±1.00	ns
CLKIN (using CLKFX outputs)	CLKIN_PER_JITT_FX_HF					±1.00		±1.00	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT					±1.00		±1.00	ns

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Output Clock Jitter

Table 32: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Clock Synthesis Period Jitter									
CLK0	CLKOUT_PER_JITT_0					±100		±100	ps
CLK90	CLKOUT_PER_JITT_90					±150		±150	ps
CLK180	CLKOUT_PER_JITT_180					±150		±150	ps
CLK270	CLKOUT_PER_JITT_270					±150		±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X					±200		±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1					±150		±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2					±300		±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX								ps

Output Clock Phase Alignment

Table 33: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Phase Offset Between CLKIN and CLKFB									
CLKIN/CLKFB	CLKIN_CLKFB_PHASE					±100		±100	ps
Phase Offset Between Any DCM Outputs									
All CLK* outputs	CLKOUT_PHASE					±140		±140	ps
Duty Cycle Precision									
DLL outputs[1]	CLKOUT_DUTY_CYCLE_DLL					±150		±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX					±100		±100	ps

Miscellaneous Timing Parameters

Table 34: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Time Required to Achieve LOCK									
Using DLL outputs[1]	LOCK_DLL								
		> 60MHz				20		20	us
		50 - 60 MHz				25		25	us
		40 - 50 MHz				50		50	us
		30 - 40 MHz				90		90	us
		24 - 30 MHz				120		120	us
Using CLKFX outputs	LOCK_FX				10 us	10	10 us	10	ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT					50		50	us
Fine Phase Shifting									
Absolute shifting range	FINE_SHIFT_RANGE					10		10	ns
Delay Lines									
Tap delay resolution	DCM_TAP				40	50	40	50	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Parameter Cross-Reference

Table 35: **Parameter Cross-Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). Values were added and revised in tables in the following sections: • **Virtex-II Performance Characteristics** • **Virtex-II Switching Characteristics** • **DCM Timing Parameters** • Table 17, “Delay Measurement Methodology,” on page 15
04/23/01	1.5	• Updated values in the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections. • Added T_{REG32} symbol to Table 21. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS031-2, Virtex-II 1.5V FPGAs: **Functional Description (Module 2)**
- DS031-3, Virtex-II 1.5V FPGAs: DC and Switching Characteristics (Module 3)
- DS031-4, Virtex-II 1.5V FPGAs: **Pinout Tables (Module 4)**