XCR5128: 128 Macrocell CPLD

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Product Specification

Features

- Industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- IEEE 1149.1-compliant, JTAG Testing Capability
  - Four pin JTAG interface (TCK, TMS, TDI, TDO)
  - IEEE 1149.1 TAP Controller
  - JTAG commands include: Bypass, Sample/Preload, Extest, Usercode, Idcode, HighZ
- 5V, In-System Programmable (ISP) using the JTAG interface
  - On-chip supervoltage generation
  - ISP commands include: Enable, Erase, Program, Verify
  - Supported by multiple ISP programming platforms
- High speed pin-to-pin delays of 7.5 ns
- Ultra-low static power of less than 100 µA
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Four clocks available
- Programmable clock polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Xilinx CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-state buffer
  - Asynchronous macrocell register preset/reset
- Programmable global 3-state pin facilitates "bed of nails" testing without using logic resources
- Available in PLCC, VQFP, and PQFP packages
- Available in both Commercial and Industrial grades

Description

The XCR5128 CPLD (Complex Programmable Logic Device) is the third in a family of CoolRunner® CPLDs from Xilinx. These devices combine high speed and zero power in a 128 macrocell CPLD. With the FZP design technique, the XCR5128 offers true pin-to-pin speeds of 7.5 ns, while simultaneously delivering power that is less than 100 µA at standby without the need for ‘turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. These devices are the first TotalCMOS PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP design technique. For 3V applications, Xilinx also offers the high-speed XCR3128 CPLD that offers these features in a full 3V implementation.

The Xilinx FZP CPLDs utilize the patented XPLA (eXtended Programmable Logic Array) architecture. The XPLA architecture combines the best features of both PLA and PAL type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA structure in each logic block provides a fast 7.5 ns PAL path with five dedicated product terms per output. This PAL path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2 ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 9.5 ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The XCR5128 CPLDs are supported by industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting

uses a Xilinx developed tool, XPLA Professional (available on the Xilinx web site).

The XCR5128 CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others. The XCR5128 also includes an industry-standard, IEEE 1149.1, JTAG interface through which in-system programming (ISP) and reprogramming of the device is supported.

XPLA Architecture

Figure 1 shows a high level block diagram of a 128 macrocell device implementing the XPLA architecture. The XPLA architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

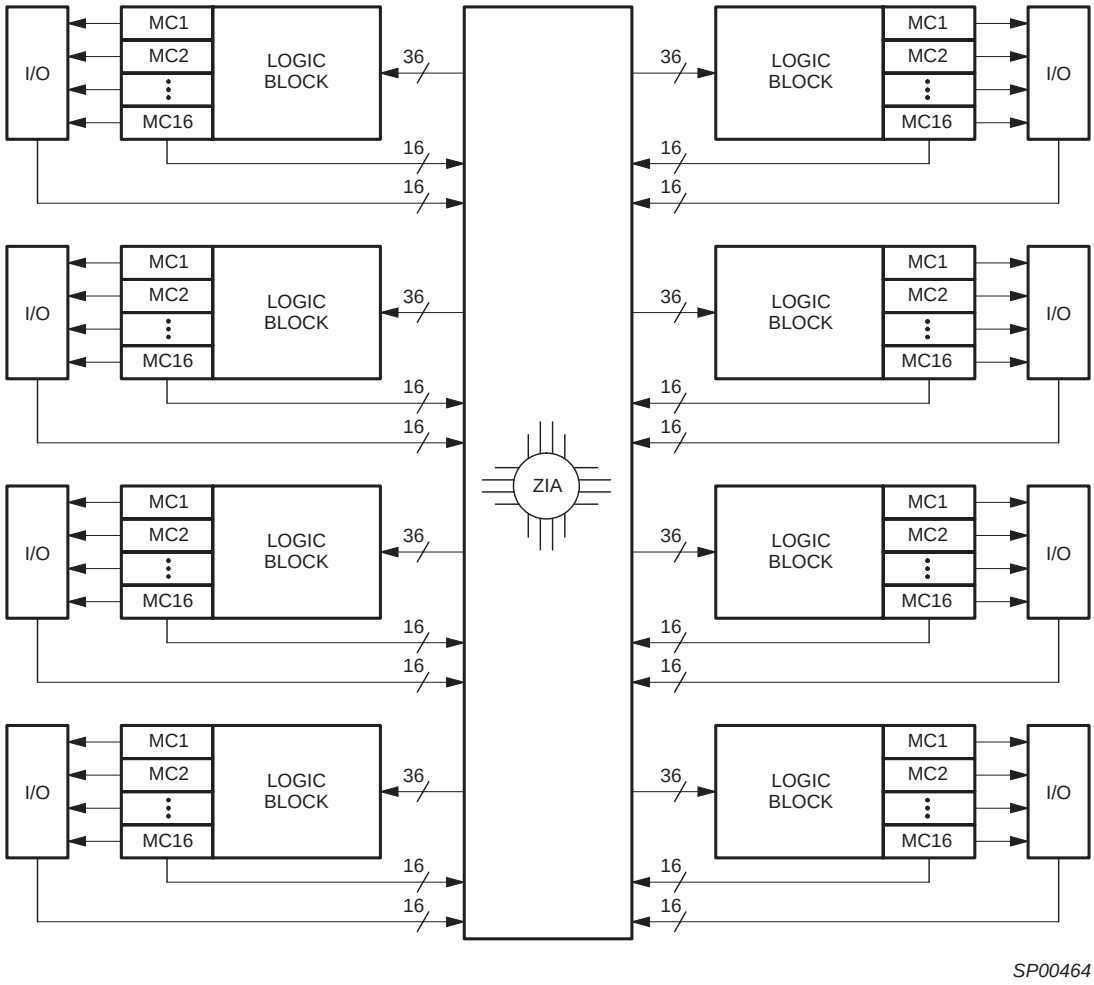

Figure 1: Xilinx XPLA CPLD Architecture

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. the six control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has five dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the XCR5128 device through the PAL array is 7.5 ns. If a macrocell needs more than five product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using one or all 32 PLA product terms is just 2 ns. So the total pin-to-pin t_{PD} for the XCR5128 using six to 37 product terms is 9.5 ns (7.5 ns for the PAL + 2 ns for the PLA)

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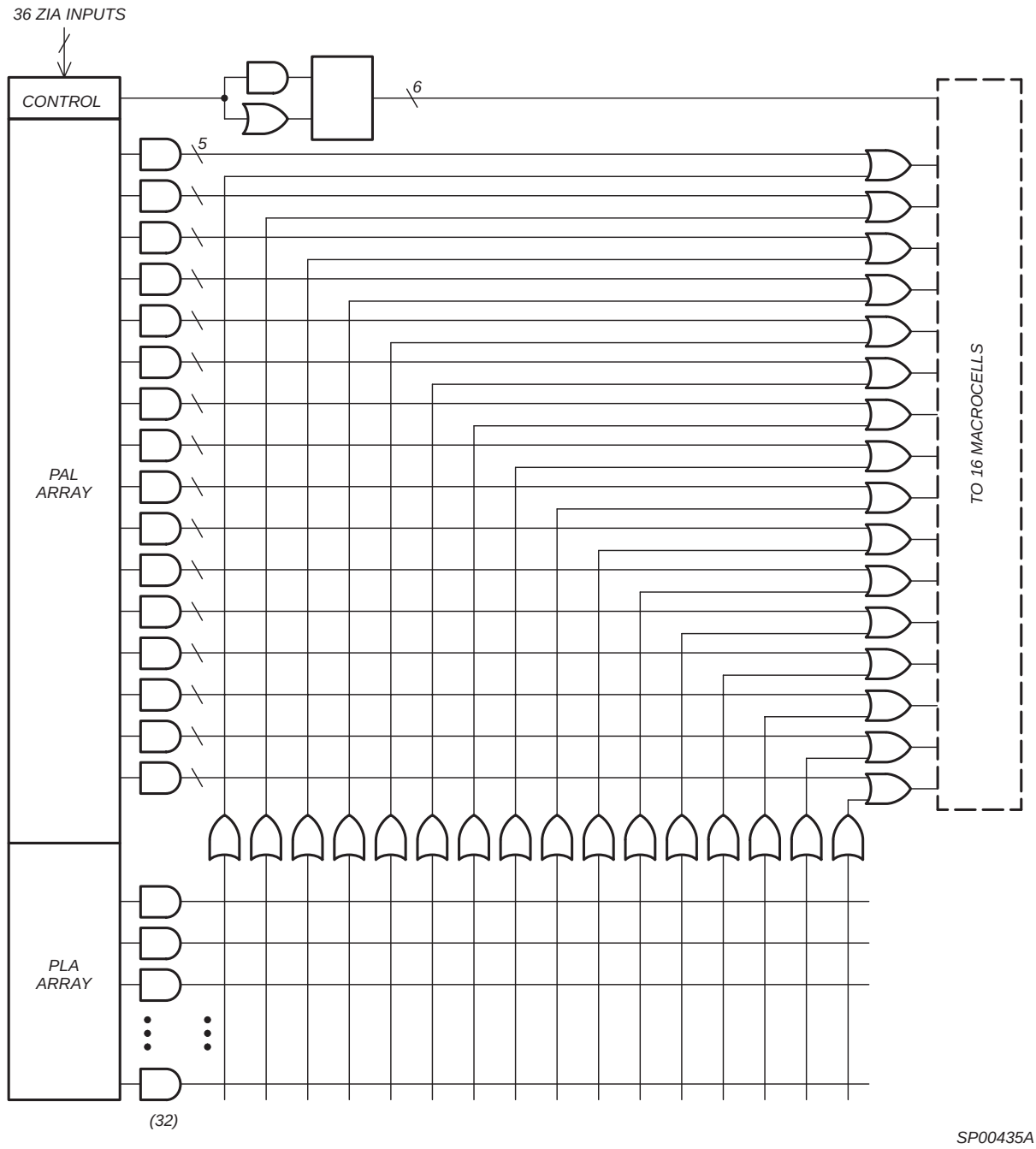


Figure 2: Xilinx XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner family. The macrocell consists of a flip-flop that can be configured as either a D- or T- type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are four clocks available on the XCR5128 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other four control terms (CT2-CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner devices also provide a Global 3-State (GTS) pin, which, when enabled and pulled Low, will 3-state all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails Testing".

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated (see the section on Terminations in this data sheet and the application note: *Terminating Unused I/O Pins in xilinx XPLA1 and XPLA2 CPLDs*).

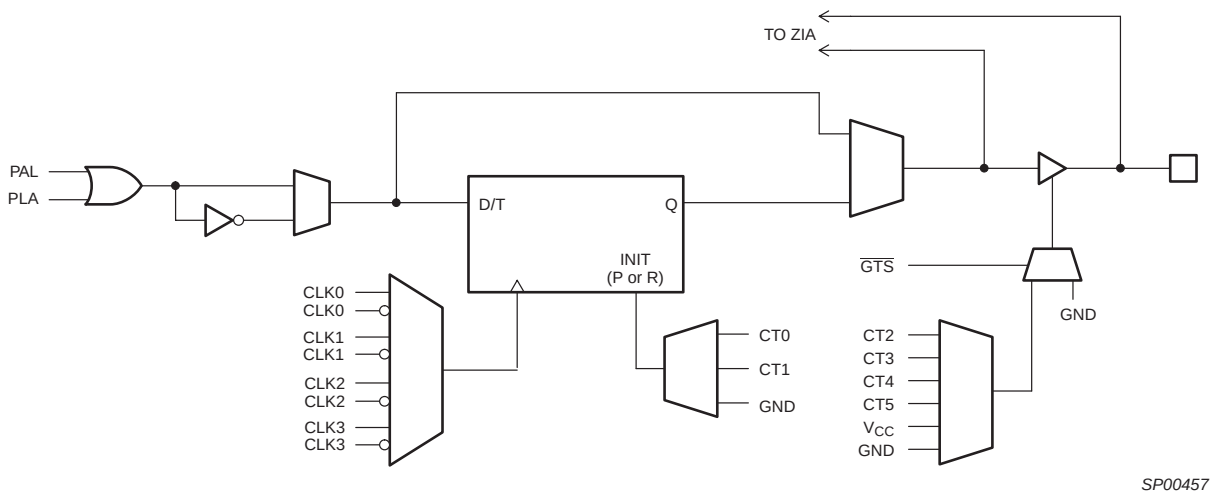


Figure 3: XCR5128 Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner Timing Model. The CoolRunner timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 1 showing the I_{CC} vs. Frequency of Xilinx' XCR5128 TotalCMOS CPLD (data taken w/eight up/down, loadable 16 bit counters at 5V, 25°C.

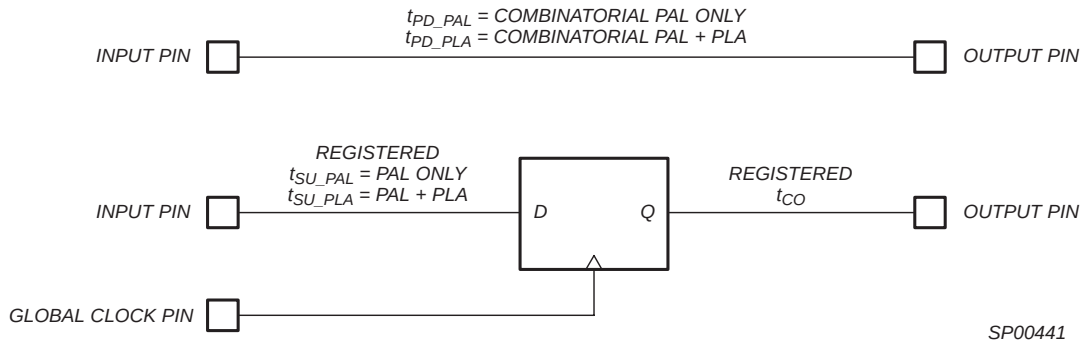


Figure 4: CoolRunner Timing Model

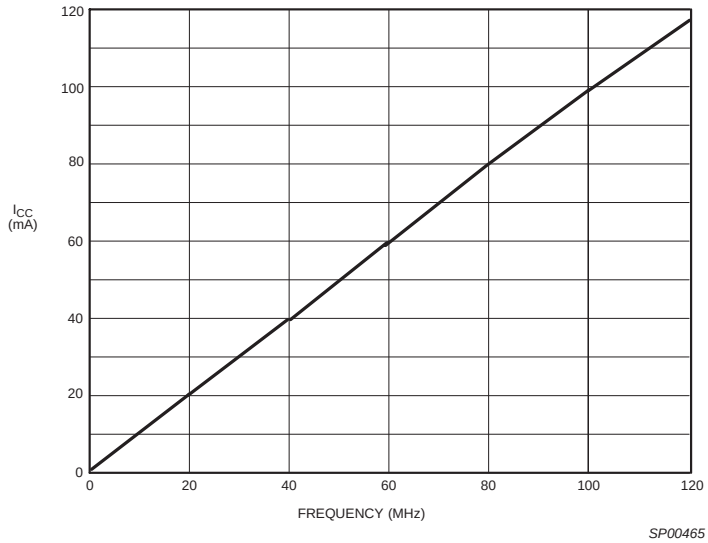


Figure 5: I_{CC} vs. Frequency at V_{CC} = 5V, 25°C

Table 1: I_{CC} vs. Frequency (V_{CC} = 5V, 25°C)

Frequency (MHz)	0	1	20	40	60	80	100	120
Typical I_{CC} (mA)	0.5	1	20	40	60	80	99	118

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
  - Enables desired signal levels to be set at specific pins (Preload)
  - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., "bed-of-nails")
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment
  - Reduces test preparation time
  - Reduces spare board inventories

The Xilinx XCR5128's JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Xilinx XCR5128, the TAP Port includes four of the five pins (refer to Table 2) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Xilinx XCR5128 saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Xilinx XCR5128 supports the test reset functionality through the use of its power up reset circuit, which is included in all Xilinx CPLDs. The pins associated with the power up reset circuit should connect to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

In the Xilinx XCR5128, the four mandatory JTAG pins each require a unique, dedicated pin on the device. However, if JTAG and ISP are not desired in the end-application, these pins may instead be used as additional general I/O pins. The decision as to whether these pins are used for JTAG/ISP or as general I/O is made when the JEDEC file is generated. If the use of JTAG/ISP is selected, the dedi-

cated pins are not available for general purpose use. However, unlike competing CPLD's, the Xilinx XCR5128 does allow the macrocell logic associated with these dedicated pins to be used as buried logic even when JTAG/ISP is selected. Table 3 defines the dedicated pins used by the four mandatory JTAG signals for each of the XCR5128 package types.

JTAG specifications define two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the Xilinx XCR5128 is defined in Table 4. By supporting this set of low-level commands, the XCR5128 allows execution of all high-level boundary-scan commands.

Table 2: JTAG Pin Description

Pin	Name	Description
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCK is also used to clock the TAP Controller state machine.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 3: XCR5128 JTAG Pinout by Package Type

Device PZ5128	(Pin Number / Macrocell #)			
	TCK	TMS	TDI	TDO
84-pin PLCC	62 / 96 (F15)	23 / 48 (C15)	14 / 32 (B15)	71 / 112 (G15)
100-pin PQFP	64 / 96 (F15)	17 / 48 (C15)	6 / 32 (B15)	75 / 112 (G15)
100-pin VQFP	62 / 96 (F15)	15 / 48 (C15)	4 / 32 (B15)	73 / 112 (G15)
128-pin TQFP	82 / 96 (F15)	21 / 48 (C15)	8 / 32 (B15)	95 / 112 (G15)
160-pin PQFP	99 / 96 (F15)	22 / 48 (C15)	9 / 32 (B15)	112/ 112 (G15)

Table 4: XCR5128 Low-Level JTAG Boundary-Scan Commands

Instruction (Instruction Code) Register Used	Description
Sample/Preload (0010) Boundary-Scan Register	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan Shift-Register prior to selection of the other boundary-scan test instructions.
Extest (0000) Boundary-Scan Register	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-Scan Shift-Register using the Sample/Preload instruction prior to selection of the EXTEST instruction.
Bypass (1111) Bypass Register	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.

Table 4: XCR5128 Low-Level JTAG Boundary-Scan Commands

Idcode (0001) Boundary-Scan Register	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HighZ (0101) Bypass Register	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HighZ instruction also forces the Bypass Register between TDI and TDO.

5V, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-Functional hardware
  - Reconfigurability for Test
  - Eliminates handling of "fine lead-pitch" components for programming
  - Reduced Inventory and manufacturing costs
  - Improved quality and reliability
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, re-configuration, and customization

The Xilinx XCR5128 allows for 5V, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided supervoltages, so that the XCR5128 may be easily programmed on the circuit board using only the 5V supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the XCR5128 enable this feature. The ISP commands implemented in the Xilinx XCR5128 are specified in Table 6. Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command **and** the device has not gone through a Test-Logic/Rest TAP Controller State.

Terminations

The CoolRunner XCR5128 CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The XCR5128 CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-downs are automatically activated by the fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. We recommend that any unused I/O pins on the XCR5128 device be left unconnected.

There are no on-chip pull-down structures associated with the dedicated input pins. Xilinx recommends that any unused dedicated inputs be terminated with external 10kΩ pull-up resistors. These pins can be directly connected to V_{CC} or GND, but using the external pull-up resistors maintains maximum design flexibility should one of the unused dedicated inputs be needed due to future design changes.

When using the JTAG/ISP functions, it is also recommended that 10kΩ pull-up resistors be used on each of the pins associated with the four mandatory JTAG signals. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times. See the application notes *JTAG and ISP Overview for Xilinx XPLA1 and XPLA2 CPLDs* and *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs* for more information.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Xilinx XCR5128 supports the following methods:

- PC parallel port
- Workstation or PC serial port
- Embedded processor
- Automated test equipment
- Third party programmers
- High-End JTAG and ISP tools

A Boundary-Scan Description Language (BSDL) description of the XCR5128 is also available from Xilinx for use in test program development. For more details on JTAG and ISP for the XCR5128, refer to the related application note: *JTAG and ISP in Xilinx CPLDs*.

Table 5: Low Level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	1001	Enables the Erase, Program, and Verify commands. Using the ENABLE instruction before the Erase, Program, and Verify instructions allows the user to specify the outputs the device using the JTAG Boundary-Scan SAMPLE/PRELOAD command.
Erase (ISP Shift Register)	1010	Erases the entire EEPROM array. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Program (ISP Shift Register)	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Verify (ISP Shift Register)	1100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.

Programming Specifications

Symbol	Parameter	Min.	Max.	Unit
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	4.5	5.5	V
I_{CCP}	I_{CC} limit program/verify		200	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{SOL}	Output voltage (Low)		0.5	V
V_{SOH}	Output voltage (High)	2.4		V
TDO_I_{OL}	Output current (Low)	12		mA
TDO_I_{OH}	Output current (High)	-12		mA
AC Parameters				
f_{MAX}	CLK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		µs
INIT	Initialization time	100		µs
TMS_SU	TMS setup time before TCK ↑	10		ns
TDI_SU	TDI setup time before TCK ↑	10		ns
TMS_H	TMS hold time after TCK ↑	20		ns
TDI_H	TDI hold time after TCK ↑	20		ns
TDO_CO	TDO valid after TCK ↓		30	ns

Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage[2]	-0.5	7.0	V
V_I	Input voltage	-1.2	V_{CC} +0.5	V
V_{OUT}	Output voltage	-0.5	V_{CC} +0.5	V
I_{IN}	Input current	-30	30	mA
I_{OUT}	Output current	-100	100	mA
T_J	Maximum junction temperature	-40	150	5C
T_{str}	Storage temperature	-65	150	5C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to +70°C	5.0V +5%
Industrial	-40 to +85°C	5.0V +10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 4.75V ≤ V_{CC} ≤ 5.25V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.75V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.25V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = -18mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.75V, I_{OL} = 12mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.75V, I_{OH} = -12mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}	Standby current	V_{CC} = 5.25V, T_{AMB} = 0°C		100	µA
I_{CCD}[2]	Dynamic current	V_{CC} = 5.25V, T_{AMB} = 0°C at 1 MHz		5	mA
		V_{CC} = 5.25V, T_{AMB} = 0°C at 50 MHz		75	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-200	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 7 for typical values.
2. his parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 4.75V ≤ V_{CC} ≤ 5.25V

Symbol	Parameter	7		10		12		Unit
		Min/	Max.	Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	2	12	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	9.5	3	12	3	14.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	6	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	4.5		7		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	6.5		9		10.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		4		ns
t_{CL}	Clock Low time	3		4		4		ns
t_R	Input Rise time		20		20		20	ns
t_F	Input Fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	167		125		125		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	111		80		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	95		71		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
$t_{PDF\_PA\ L}$	Input (or feedback node) to internal feedback node delay time through PAL	2	6	2	8.5	2	10.5	ns
$t_{PDF\_PL\ A}$	Input (or feedback node) to internal feedback node delay time through PAL+ PLA	3	8	3	10.5	3	13	ns
t_{CF}	Clock to internal feedback node delay time		4.5		5.5		6.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50		50	µs
t_{ER}	Input to output disable[2, 3]		9		12		15	ns
t_{EA}	Input to output valid[2]		9		12		15	ns
t_{RP}	Input to register preset[2]		11		12.5		15	ns
t_{RR}	Input to register reset[2]		11		12.5		15	ns

Notes:

1. Specifications measured with one output switching. See Figure 6 and Table 6 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output c_l = 5 pf.

DC Electrical Characteristics For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.5V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.5V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.5V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.5V, I_{OL} = 12 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.5V, I_{OH} = -12 mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 5.5V, T_{AMB} = -40°C		125	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 5.5V, T_{AMB} = -40°C at 1 MHz		6	mA
		V_{CC} = 5.5V, T_{AMB} = -40°C at 50 MHz		90	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-230	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 7 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics For Industrial Grade Devices

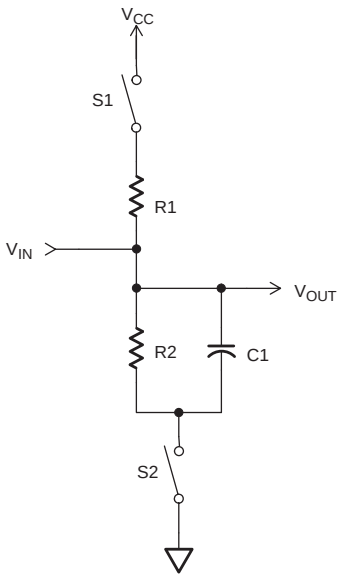
Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

Symbol	Parameter	10		15		Unit
		Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	15	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	12	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	8		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	10		10.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	5		5		ns
t_{CL}	Clock Low time	5		5		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	100		100		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	71		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	66		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	8.5	2	13.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+ PLA	3	10.5	3	16	ns
t_{CF}	Clock to internal feedback node delay time		6		6.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		15		15	ns
t_{EA}	Input to output valid[2]		15		15	ns
t_{RP}	Input to register preset[2]		15		17	ns
t_{RR}	Input to register reset[2]		15		17	ns

Notes:

1. Specifications measured with one output switching. See Figure 6 and Table 6 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

Switching Characteristics



COMPONENT	VALUES
R1	470Ω
R2	250Ω
C1	35 pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_P	Closed	Closed

Note: For t_{PHZ} and t_{PLZ} C = 5 pF.

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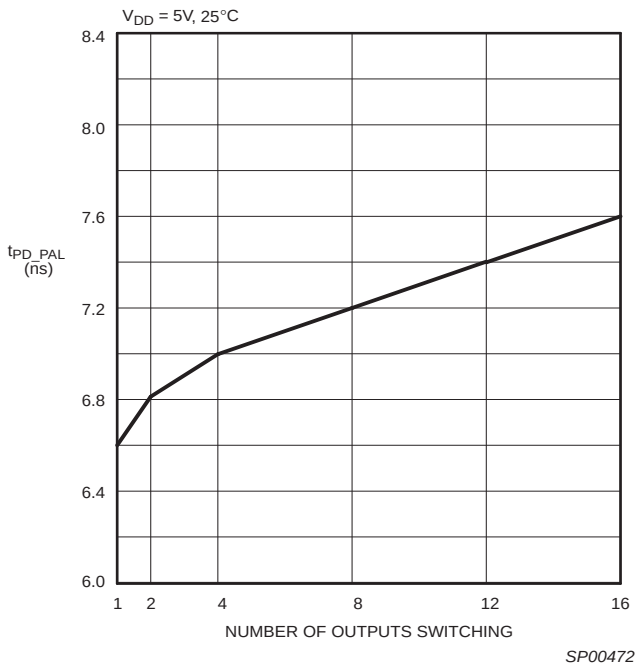

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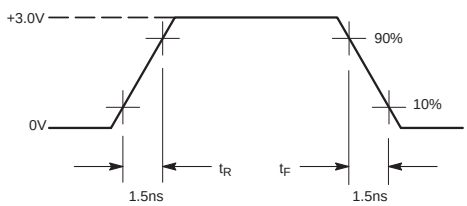
Figure 6: t_{PD_PAL} vs. Outputs Switching

Voltage Waveform



SP00368

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Table 6: t_{PD_PAL} vs. Number of Outputs Switching
(VCC = 5V)

Number Of Outputs	1	2	4	8	12	16
Typical (ns)	6.6	6.8	7.0	7.2	7.4	7.6

Pin Function and Layout

XCR5128 I/O Pins

Function Block	Macrocell	PC84	PQ100	VQ100	TQ128	PQ160	Notes
1	1	-	4	2	3	160	
1	2	-	-	-	-	-	
1	3	12	3	1	2	159	
1	4	-	-	-	1	158	
1	5	11	2	100	128	153	
1	6	10	1	99	127	152	
1	7	-	-	-	-	-	
1	8	9	100	98	126	151	
1	9	-	99	97	125	150	
1	10	-	-	-	-	-	
1	11	8	98	96	124	149	
1	12	-	-	-	122	147	
1	13	6	96	94	121	146	
1	14	5	95	93	120	145	
1	15	-	-	-	-	-	
1	16	4	94	92	119	144	
2	1	22	16	14	20	21	
2	2	-	-	-	-	-	
2	3	21	15	13	19	20	
2	4	-	-	-	18	19	
2	5	20	14	12	17	18	
2	6	-	12	10	15	16	
2	7	-	-	-	-	-	
2	8	18	11	9	14	15	
2	9	17	10	8	13	14	
2	10	-	-	-	-	-	
2	11	16	9	7	12	13	
2	12	-	-	-	11	12	
2	13	15	8	6	10	11	
2	14	-	7	5	9	10	
2	15	-	-	-	-	-	
2	16	14	6	4	8	9	(1)
3	1	-	27	25	36	41	
3	2	-	-	-	-	-	
3	3	31	26	24	32	33	
3	4	-	-	-	31	32	
3	5	30	25	23	30	31	
3	6	29	24	22	29	30	
3	7	-	-	-	-	-	
3	8	28	23	21	28	29	
3	9	-	22	20	27	28	
3	10	-	-	-	-	-	
3	11	27	54	19	26	27	
3	12	-	-	-	24	25	
3	13	25	19	17	23	24	
3	14	24	18	16	22	23	
3	15	-	-	-	-	-	
3	16	23	17	15	21	22	(1)
4	1	41	39	37	50	59	
4	2	-	-	-	-	-	
4	3	40	38	36	49	58	
4	4	-	-	-	48	57	
4	5	39	37	35	47	56	
4	6	-	35	33	45	54	
4	7	-	-	-	-	-	
4	8	37	34	32	44	53	
4	9	36	33	31	43	52	
4	10	-	-	-	-	-	
4	11	35	32	30	42	51	
4	12	-	-	-	41	50	
4	13	34	31	29	40	49	
4	14	-	30	28	39	48	
4	15	-	-	-	-	-	
4	16	33	29	27	38	43	
5	1	44	42	40	53	62	
5	2	-	-	-	-	-	
5	3	45	43	41	54	63	
5	4	-	-	-	55	64	
5	5	46	44	42	56	65	
5	6	-	46	44	58	67	
5	7	-	-	-	-	-	
5	8	48	47	45	59	68	
5	9	49	48	46	60	69	
5	10	-	-	-	-	-	
5	11	50	49	47	61	70	
5	12	-	-	-	62	71	
5	13	51	50	48	63	72	
5	14	-	51	49	64	73	
5	15	-	-	-	-	-	
5	16	52	52	50	65	78	
6	1	-	54	52	67	80	
6	2	-	-	-	-	-	
6	3	54	55	53	71	88	
6	4	-	-	-	72	89	
6	5	55	56	54	73	90	
6	6	56	57	55	74	91	
6	7	-	-	-	-	-	
6	8	57	58	56	75	92	
6	9	-	59	57	76	93	
6	10	-	-	-	-	-	
6	11	58	60	58	77	94	
6	12	-	-	-	79	96	
6	13	60	62	60	80	97	

Function Block	Macrocell	PC84	PQ100	VQ100	TQ128	PQ160	Notes
6	14	61	63	61	81	98	
6	15	-	-	-	-	-	
6	16	62	64	62	82	99	(1)
7	1	63	65	63	83	100	
7	2	-	-	-	-	-	
7	3	64	66	64	84	101	
7	4	-	-	-	85	102	
7	5	65	67	65	86	103	
7	6	-	69	67	88	104	
7	7	-	-	-	-	-	
7	8	67	70	68	89	105	
7	9	68	71	69	90	106	
7	10	-	-	-	-	-	
7	11	69	72	70	91	107	
7	12	-	-	-	92	109	
7	13	70	73	71	93	110	
7	14	-	74	72	94	111	
7	15	-	-	-	-	-	
7	16	71	75	73	95	112	(1)
8	1	-	77	75	100	121	
8	2	-	-	-	-	-	
8	3	73	78	76	101	122	
8	4	-	-	-	102	123	
8	5	74	79	77	103	128	
8	6	75	80	78	104	129	
8	7	-	-	-	-	-	
8	8	76	81	79	105	130	
8	9	-	82	80	106	131	
8	10	-	-	-	-	-	
8	11	77	83	81	107	132	
8	12	-	-	-	109	134	
8	13	79	85	83	110	135	
8	14	80	86	84	111	136	
8	15	-	-	-	-	-	
8	16	81	87	85	112	137	

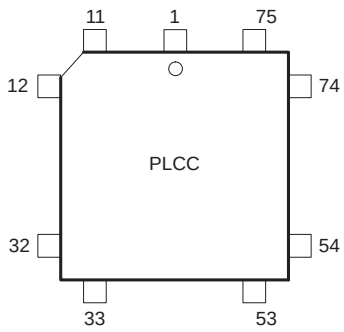
(1) JTAG pins

XCR5128 Global, JTAG, Power, Ground, and No connect Pins

Pin Type	PC84	PQ100	VQ100	TQ128	PQ160	Notes
IN0	83	89	87	114	139	
IN1	1	91	89	116	141	
IN2	84	90	88	115	140	
IN3	2	92	90	117	143	
gtsn	84	90	88	115	140	(1)
CLK0	83	89	87	114	139	
CLK1	44	42	40	53	62	
CLK2	41	39	37	50	59	
CLK3	4	94	92	119	144	
TCK	62	64	62	82	99	
TDI	14	6	4	8	9	
TDO	71	75	73	95	112	
TMS	23	17	15	21	22	
Vcc	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	3, 18, 34, 39, 51, 66, 82, 91	7, 25, 46, 52, 66, 87, 108, 118	8, 26, 55, 61, 79, 104, 133, 143	
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86, 95	16, 37, 51, 57, 78, 96, 113, 123	17, 42, 60, 66, 95, 113, 138, 148	
No Connects	-	-	-	4, 5, 6, 33, 34, 35, 68, 69, 70, 97, 98, 99	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157	

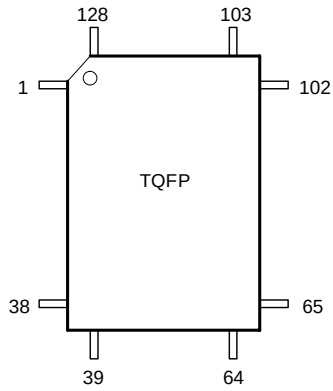
(1) Global 3-State pin facilitates bed of nails testing without using logic resources.

84-pin PLCC



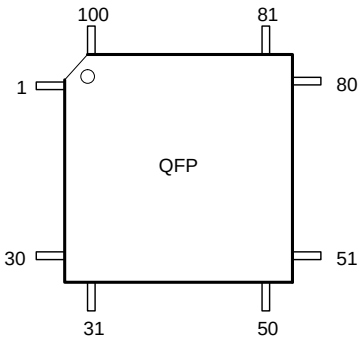
SP00467A

128-pin TQFP



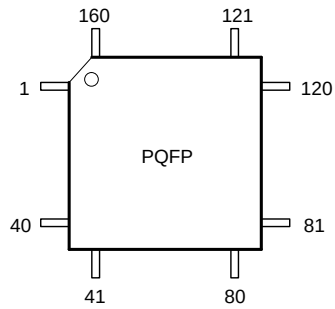
SP00469B

100-pin PQFP



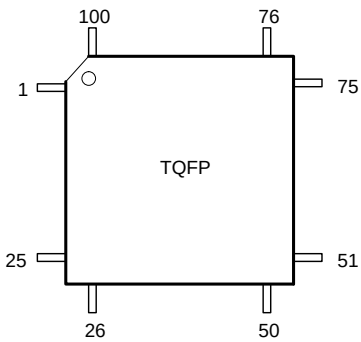
SP00468A

160-Pin PQFP



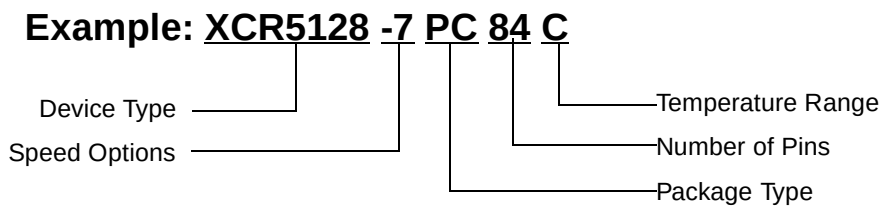
SP00470B

100-pin VQFP



SP00485A

Ordering Information



Speed Options
-15: 15 ns pin-to-pin delay
-12: 12 ns pin-to-pin delay
-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
PC84: 84-pin PLCC
PQ100: 100-pin PQFP
VQ100: 100-pin VQFP
TQ128: 128-pin TQFP
PQ160: 160-pin PQFP

Component Availability

Pins		84	100		128	160
Type		Plastic PLCC	Plastic PQFP	Plastic VQFP	Plastic TQFP	Plastic PQFP
Code		PC84	PQ100	VQ100	TQ128	PQ160
XCR5128	-15	I	I	I	I	I
	-12	C	C	C	C	C
	-10	C, I	C, I	C, I	C, I	C, I
	-7	C	C	C	C	C

Revision History

Date	Version #	Revision
9/16/99	1.0	Initial Xilinx release.
2/10/00	1.1	Coverted to Xilinx format and updated.
8/10/00	1.2	Updated features and pinout tables.
10/09/00	1.3	Added Discontinuation Notice.
01/19/01	1.4	Added pin descriptions to PC84 package to VCC and GND.