XC9572XV High-performance CPLD

DS052 (v2.0) January 29, 2001

Advance Product Specification

Features

- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (38 user I/O pins)
  - 100-pin TQFP (72-user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Two separate output banks
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95144XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 4 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

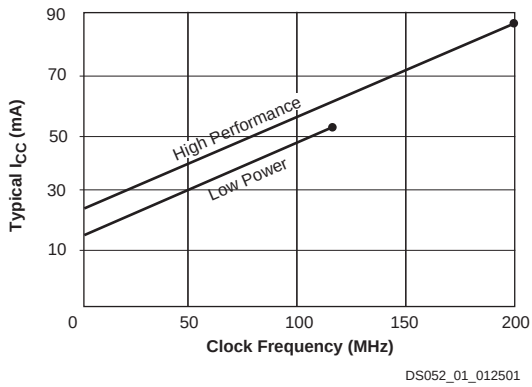


Figure 1: **Typical I_{CC} vs. Frequency for XC9572XV**

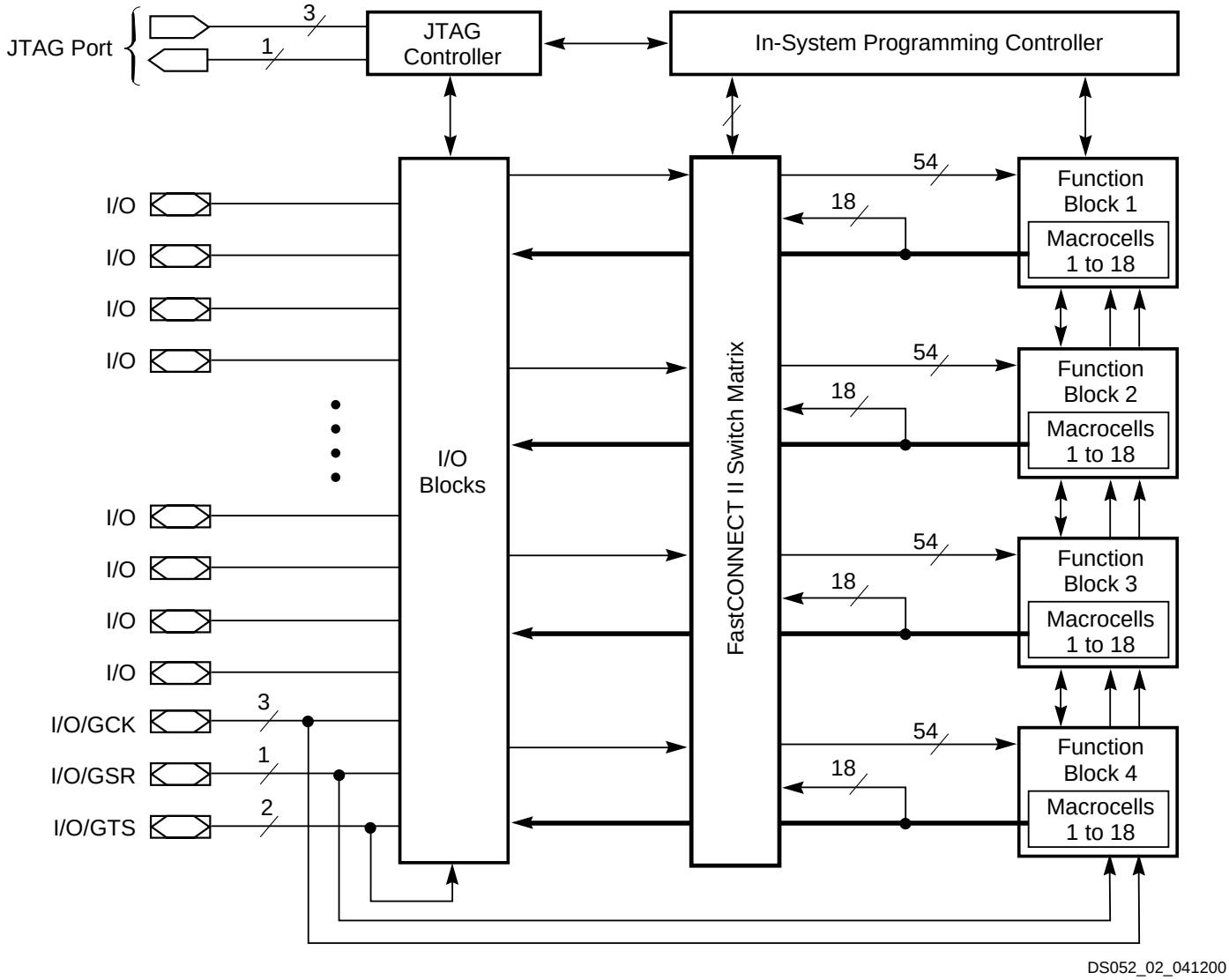


Figure 2: **XC9572XV Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 2.7	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 3.6	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	2.4	2.6	V
		Industrial T_A = –40°C to +85°C	2.4	2.6	
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.1	3.5	V
	Supply voltage for output drivers for 2.5V operation		2.4	2.6	V
	Supply voltage for output drivers for 1.8V operation		1.7	1.9	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		1.7	3.6	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase cycles (endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

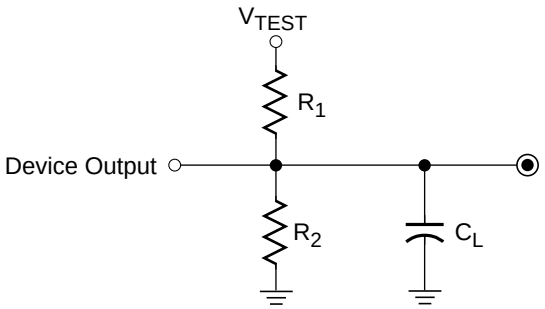
DC Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –1.0 mA	2.0	-	V
	Output high voltage for 1.8V outputs	I_{OH} = –100 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 1.0 mA	-	0.4	V
	Output low voltage for 1.8V outputs	I_{OL} = 100 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = 2.6V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = 2.0V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	10	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	14		mA

AC Characteristics

Symbol	Parameter	XC9572XV-4		XC9572XV-5		XC9572XV-7		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	4.0	-	5.0	-	7.5	ns
T_{SU}	I/O setup time before GCK	3.1	-	3.7	-	4.8	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	2.0	-	2.5	-	4.5	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	250.0	-	222.2	-	125.0	MHz
T_{PSU}	I/O setup time before p-term clock input	0.5	-	0.7	-	1.6	-	ns
T_{PH}	I/O hold time after p-term clock input	1.8	-	2.0	-	3.2	-	ns
T_{PCO}	P-term clock output valid	-	4.6	-	5.5	-	7.7	ns
T_{OE}	GTS to output valid	-	2.5	-	3.0	-	5.0	ns
T_{OD}	GTS to output disable	-	2.5	-	3.0	-	5.0	ns
T_{POE}	Product term OE to output enabled	-	5.5	-	7.0	-	9.5	ns
T_{POD}	Product term OE to output disabled	-	5.5	-	7.0	-	9.5	ns
T_{AO}	GSR to output valid	-	7.7	-	10.0	-	12.0	ns
T_{PAO}	P-term S/R to output valid	-	8.5	-	10.5	-	12.6	ns
T_{WLH}	GCK pulse width (High or Low)	2.0	-	2.2	-	4.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	5.0	-	6.5	-	ns
		Advance Information						

Notes:
1. Please contact Xilinx for up-to-date information on advance specifications.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320Ω	360Ω	35 pF
	2.5V	2.5V	250Ω	660Ω	35 pF
	1.8V	1.8V	10KΩ	14KΩ	35 pF

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Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC9572XV-4		XC9572XV-5		XC9572XV-7		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.2	-	1.5	-	2.3	ns
T_{GCK}	GCK buffer delay	-	0.2	-	0.3	-	1.5	ns
T_{GSR}	GSR buffer delay	-	1.2	-	2.0	-	3.1	ns
T_{GTS}	GTS buffer delay	-	2.5	-	3.0	-	5.0	ns
T_{OUT}	Output buffer delay	-	1.6	-	2.0	-	2.5	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	1.6	-	1.8	-	2.4	ns
T_{PTSR}	Product term set/reset delay	-	0.8	-	1.0	-	1.4	ns
T_{PTTS}	Product term 3-state delay	-	4.3	-	5.5	-	7.2	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.4	-	0.5	-	1.3	ns
T_{SUI}	Register setup time	1.3	-	1.5	-	2.6	-	ns
T_{HI}	Register hold time	1.0	-	1.2	-	2.2	-	ns
T_{ECSU}	Register clock enable setup time	1.3	-	1.5	-	2.6	-	ns
T_{ECHO}	Register clock enable hold time	1.0	-	1.2	-	2.2	-	ns
T_{COI}	Register clock to output valid time	-	0.2	-	0.2	-	0.5	ns
T_{AOI}	Register async. S/R to output delay	-	4.9	-	6.0	-	6.4	ns
T_{RAI}	Register async. S/R recover before clock	4.0		5.0		7.5		ns
T_{LOGI}	Internal logic delay	-	0.8	-	1.0	-	1.4	ns
T_{LOGILP}	Internal low power logic delay	-	3.8	-	5.0	-	6.4	ns
Feedback Delays								
T_F	FastCONNECT II™ feedback delay	-	1.7	-	1.8	-	3.5	ns
Time Adders								
T_{PTA}	Incremental product term allocator delay	-	0.6	-	0.7	-	0.8	ns
T_{PTA2}	Adjacent macrocell p-term allocator delay	-	0.2	-	0.3	-	0.3	ns
T_{SLEW}	Slew-rate limited delay	-	2.5	-	3.0	-	4.0	ns
		Advance Information						

Notes:
1. Please contact Xilinx for up-to-date information on advance specifications.

XC9572XV I/O Pins

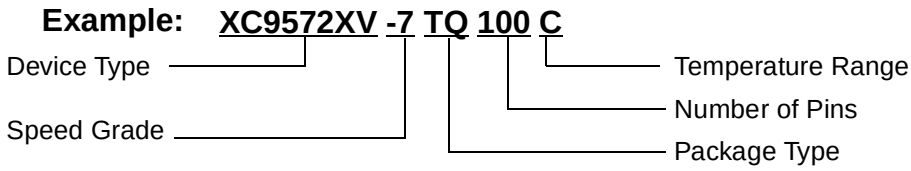
Function Block	Macro-cell	PC44	VQ44	CS48	TQ100	BScan Order	Function Block	Macro-cell	PC44	VQ44	CS48	TQ100	BScan Order
1	1	-	-	-	16	213	3	1	-	-	-	41	105
1	2	1	39	D7	13	210	3	2	11	5	B5	32	102
1	3	-	-	D4	18	207	3	3	-	-	C4	49	99
1	4	-	-	-	20	204	3	4	-	-	-	50	96
1	5	2	40	D6	14	201	3	5	12	6	A4	35	93
1	6	3	41	C7	15	198	3	6	-	-	-	53	90
1	7	-	-	-	25	195	3	7	-	-	-	54	87
1	8	4	42	C6	17	192	3	8	13	7	B4	37	84
1	9	5(1)	43(1)	B7(1)	22(1)	189	3	9	14	8	A3	42	81
1	10	-	-	-	28	186	3	10	-	-	D3	60	78
1	11	6(1)	44(1)	B6(1)	23(1)	183	3	11	18	12	B2	52	75
1	12	-	-	-	33	180	3	12	-	-	-	61	72
1	13	-	-	-	36	177	3	13	-	-	-	63	69
1	14	7(1)	1(1)	A7(1)	27(1)	174	3	14	19	13	B1	55	66
1	15	8	2	A6	29	171	3	15	20	14	C2	56	63
1	16	-	-	-	39	168	3	16	24	18	D2	64	60
1	17	9	3	C5	30	165	3	17	22	16	C3	58	57
1	18	-	-	-	40	162	3	18	-	-	-	59	54
2	1	-	-	-	87	159	4	1	-	-	-	65	51
2	2	35	29	F4	94	156	4	2	25	19	E1	67	48
2	3	-	-	-	91	153	4	3	-	-	-	71	45
2	4	-	-	-	93	150	4	4	-	-	-	72	42
2	5	36	30	G5	95	147	4	5	26	20	E2	68	39
2	6	37	31	F5	96	144	4	6	-	-	E4	76	36
2	7	-	-	-	3(2)	141	4	7	-	-	-	77	33
2	8	38	32	G6	97	138	4	8	27	21	F1	70	30
2	9	39(1)	33(1)	G7(1)	99(1)	135	4	9	-	-	-	66	27
2	10	-	-	-	1	132	4	10	-	-	-	81	24
2	11	40(1)	34(1)	F6(1)	4(1)	129	4	11	28	22	G1	74	21
2	12	-	-	-	6	126	4	12	-	-	-	82	18
2	13	-	-	-	8	123	4	13	-	-	-	85	15
2	14	42(3)	36(3)	E6(3)	9(3)	120	4	14	29	23	F2	78	12
2	15	43	37	E7	11	117	4	15	33	27	E3	89	9
2	16	-	-	-	10	114	4	16	-	-	-	86	6
2	17	44	38	E5	12	111	4	17	34	28	G4	90	3
2	18	-	-	-	92	108	4	18	-	-	-	79	0

Notes:
1. Global control pin.
2. GTS1 for TQ100
3. GTS1 for PC44, CS48, VQ44

XC9572XV Global, JTAG and Power Pins

Pin Type	PC44	VQ44	CS48	TQ100
I/O/GCK1	5	43	B7	22
I/O/GCK2	6	44	B6	23
I/O/GCK3	7	1	A7	27
I/O/GTS1	42	36	E6	3
I/O/GTS2	40	34	F6	4
I/O/GSR	39	33	G7	99
TCK	17	11	A1	48
TDI	15	9	B3	45
TDO	30	24	G2	83
TMS	16	10	A2	47
V_{CCINT} 2.5V	21, 41	15, 35	C1, F7	5, 57, 98
V_{CCIO} 1.8/2.5V/3.3V	32	26	G3	26, 38, 51, 88
GND	10, 23, 31	4, 17, 25	A5, D1, F3	21, 31, 44, 62, 69, 75, 84, 100
No Connects	-	-	-	2, 7, 19, 24, 34, 43, 46, 73, 80

Ordering Information



Device Ordering Options

Speed	
-7	7.5 ns pin-to-pin delay
-5	5 ns pin-to-pin delay
-4	4 ns pin-to-pin delay

Package	
PC44	44-pin Plastic Lead Chip Carrier (PLCC)
VQ44	44-pin Very Thin Quad Flat Pack (VQFP)
CS48	48-ball Chip Scale Package (CSP)
TQ100	100-pin Thin Quad Flat Pack (TQFP)

Temperature	
C = Commercial	T_A = 0°C to +70°C
I = Industrial	T_A = –40°C to +85°C

Component Availability

Pins		44	44	48	100
Type		Plastic PLCC	Plastic VQFP	Plastic CSP	Plastic TQFP
Code		PC44	VQ44	CS48	TQ100
XC9572XV	-7	C, I	C, I	C, I	C, I
	-5	C	C	C	C
	-4	(C)	(C)	-	(C)

Notes:
1. C = Commercial (T_A = 0°C to +70°C); I = Industrial (T_A = –40°C to +85°C).
2. ( ) Parenthesis indicate future planned products. Please contact Xilinx for up-to-date information.

Revision History

Date	Revision No.	Description
02/01/00	1.1	Initial Xilinx release. Advance information specification.
01/29/01	2.0	Added -4 performance specification and VQ44 pagkage. Deleted VQ64 package. Updated I_{CC} vs. Frequency Figure 1.