Spartan-II Family of One-Time Programmable Configuration PROMs (XC17S00A)

DS078 (v1.2) April 7, 2001

Advance Product Specification

Introduction

The Spartan®-II family of PROMs provide an easy-to-use, cost-effective method for storing Spartan-II device configuration bitstreams.

When the Spartan-II device is in Master Serial mode, it generates a configuration clock that drives the Spartan-II PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan-II device D_{IN} pin. The Spartan-II device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan-II device is in Slave Serial mode, the PROM and the Spartan-II device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan-II device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan-II PROM Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan-II FPGA devices
- Simple interface to the Spartan-II device
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- 3.3V PROM
- Available in compact plastic 8-pin DIP, 8-pin VOIC, 20-pin SOIC, or 44-pin VQFP packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.
- Guaranteed 20 year life data retention

Spartan-II FPGA	Configuration Bits	Compatible Spartan-II PROM
XC2S15	197,696	XC17S15A
XC2S30	336,768	XC17S30A
XC2S50	559,200	XC17S50A
XC2S100	781,216	XC17S100A
XC2S150	1,040,096	XC17S150A
XC2S200	1,335,840	XC17S200A

Pin Description

Table 1: **Spartan-II PROM Pinouts**

Pin Name	8-pin PDIP and VOIC	20-pin SOIC	44-pin VQFP	Pin Description
DATA	1	1	40	Data output, High-Z state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	43	Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	13	When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be connected to the FPGAs $\overline{INIT}$ pin and a pull-up resistor. The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.
CE	4	10	15	When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.
GND	5	11	18, 41	GND is the ground connection.
V_{CC}	7, 8	18, 20	38	The V_{CC} pins are to be connected to the positive voltage supply.

Controlling PROMs

Connecting the Spartan-II device with the PROM:

- The DATA output of the PROM drives the D_{IN} input of the lead Spartan-II device.
- The Master Spartan-II device CCLK output drives the CLK input of the PROM.
- The $\overline{RESET}$/OE input of the PROM is connected to the $\overline{INIT}$ pin of the Spartan-II device and a pull-up resistor. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The $\overline{CE}$ input of the PROM is connected to the DONE pin of the Spartan-II device and a pull-up resistor. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan-II device mode pins. In Master Serial mode, the Spartan-II device automatically loads the configuration program from an external memory. The Spartan-II PROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan-II device enters the Master Serial mode when the mode pins are set to Master Serial mode. Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface (Figure 1). Only a serial data line, two control lines, and a clock line are required to configure the Spartan-II device. Data from the PROM is read sequentially, accessed via the

internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the Spartan-II device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan-II family takes care of this automatically with an on-chip pull-up/down resistor or keeper circuit.

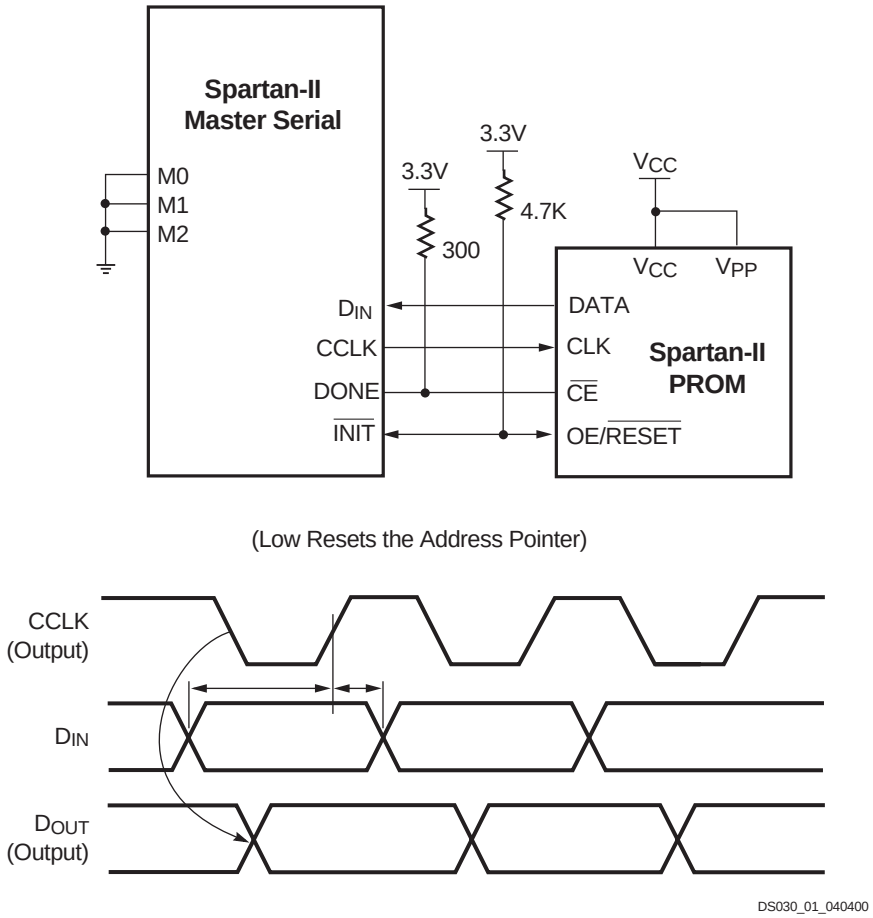


Figure 1: **Master Serial Mode.** The one-time-programmable Spartan-II PROM supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan-II FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Programming the Spartan-II Family PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

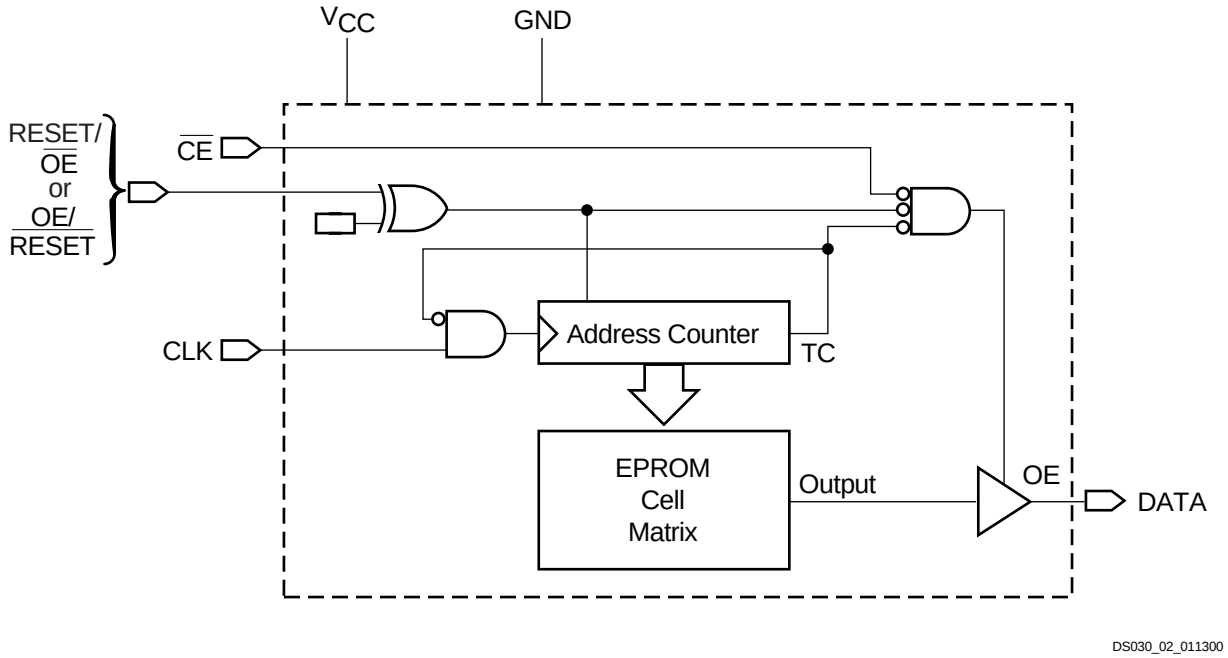


Figure 2: **Simplified Block Diagram (does not show programming circuit)**

Important: Always tie the two V_{CC} pins together in your application.

Table 2: **Truth Table for XC17S00A Control Inputs**

Control Inputs		Internal Address(2)	Outputs	
RESET(1)	CE		DATA	I_{CC}
Inactive	Low	If address ≤ TC: increment If address > TC: don't change	Active High-Z	Active Reduced
Active	Low	Held reset	High-Z	Active
Inactive	High	Not changing	High-Z	Standby
Active	High	Held reset	High-Z	Standby

Notes:
1. The XC17S00A RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

XC17S15A, XC17S30A, XC17S50A, XC17S100A, XC17S150A, XC17S200A

Absolute Maximum Ratings(1)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions(1)

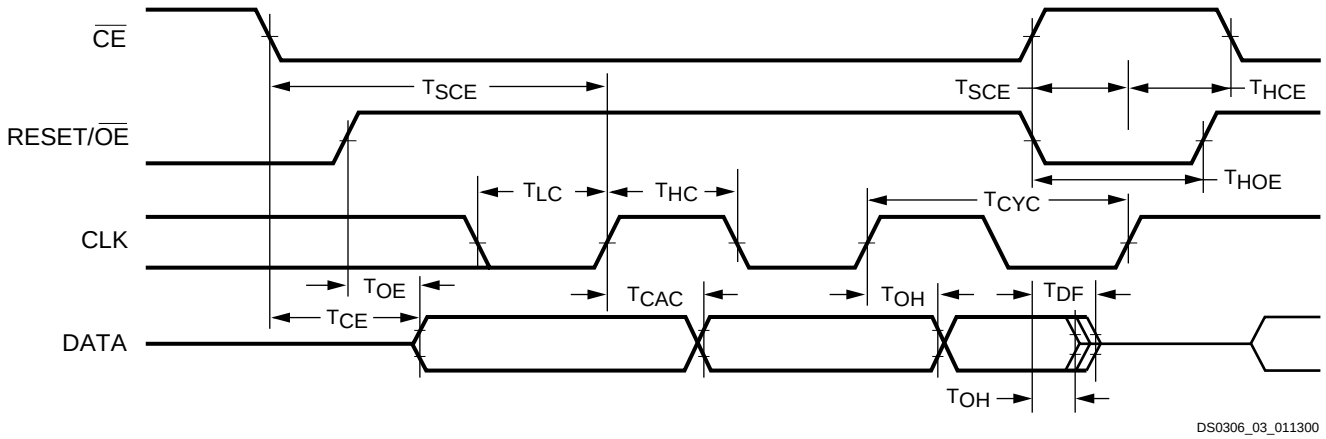
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = –40°C to +85°C)	3.0	3.6	V

Notes:
1. During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	-	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)	-	5	mA
I_{CCS}	Supply current, standby mode	-	50	µA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF

AC Characteristics Over Operating Condition(1)



Symbol	Description	Min	Max	Units
T_{OE}	RESET/$\overline{OE}$ to Data Delay	-	45	ns
T_{CE}	$\overline{CE}$ to Data Delay	-	60	ns
T_{CAC}	CLK to Data Delay	-	80	ns
T_{OH}	Data Hold From $\overline{CE}$, RESET/$\overline{OE}$, or CLK(2)	0	-	ns
T_{DF}	$\overline{CE}$ or RESET/$\overline{OE}$ to Data Float Delay(2,3)	-	50	ns
T_{CYC}	Clock Periods	100	-	ns
T_{LC}	CLK Low Time(2)	50	-	ns
T_{HC}	CLK High Time(2)	50	-	ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25	-	ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	-	ns
T_{HOE}	RESET/$\overline{OE}$ Hold Time (guarantees counters are reset)	25	-	ns

Notes:
1. AC test load = 50 pF
2. Guaranteed by design, not tested.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

XC17S15A VO8 C

Device Number

XC17S15A
XC17S30A
XC17S50A
XC17S100A
XC17S150A
XC17S200A

Package Type

PD8 = 8-pin Plastic DIP
VO8 = 8-pin Plastic Small-Outline Thin Package
SO20 = 20-pin Plastic Small-Outline Package
VQ44 = 44-pin Plastic Quad Flat Package

Operating Range/Processing

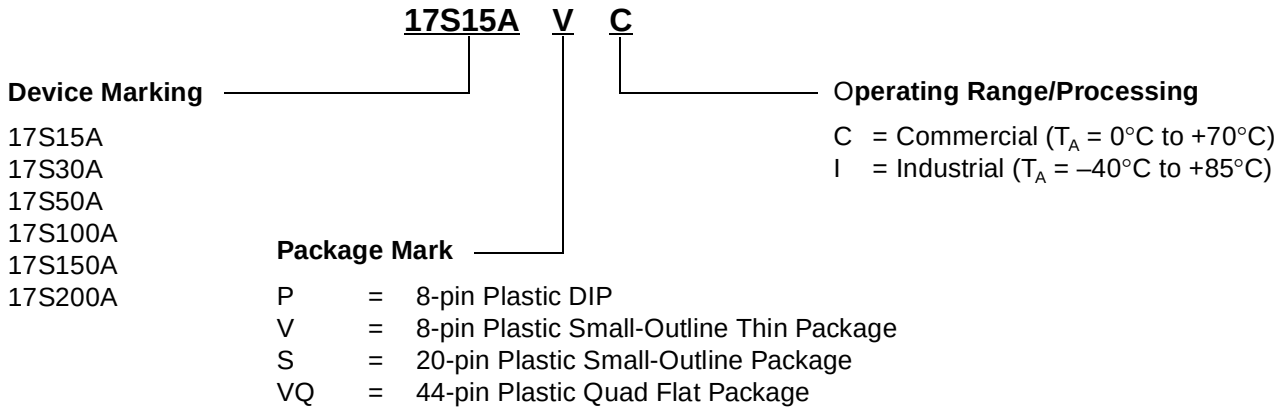
C = Commercial (T_A = 0°C to +70°C)
I = Industrial (T_A = –40°C to +85°C)

Spartan-II 3.3V Valid Ordering Combinations

XC17S15APD8C	XC17S50APD8C	XC17S150APD8C
XC17S15AVO8C	XC17S50AVO8C	XC17S150AVO8C
XC17S15ASO20C	XC17S50ASO20C	XC17S150ASO20C
XC17S15APD8I	XC17S50APD8I	XC17S150APD8I
XC17S15APD8I	XC17S50AVO8I	XC17S150AVO8I
XC17S15AVO8I	XC17S50ASO20I	XC17S150ASO20I
XC17S30APD8C	XC17S100APD8C	XC17S200APD8C
XC17S30AVO8C	XC17S100AVO8C	XC17S200AVO8C
XC17S30ASO20C	XC17S100ASO20C	XC17S200AVQ44C
XC17S30APD8I	XC17S100APD8I	XC17S200APD8I
XC17S30AVO8I	XC17S100AVO8I	XC17S200AVO8I
XC17S30ASO20I	XC17S100ASO20I	XC17S200AVQ44I

Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



Revision History

The following table shows the revision history for this document.

Date	Revision	Revision
09/14/00	1.0	Initial Xilinx release.
11/13/00	1.1	Updated configuration bits.
04/07/01	1.2	Added to features: "Guaranteed 20 year life data retention", removed "Programming the FPGA with counters" and related text.