Xilinx HardWire™ Product Family Overview

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Introduction

HardWire software and silicon provide a simple, turnkey path, used for reducing the cost of FPGA designs. When a system incorporating Xilinx FPGA's moves to high volume production, HardWire products should be the first consideration for cost reduction. HardWire products are developed specifically to be pin compatible replacements of Xilinx FPGAs. The HardWire conversion flow coupled with the HardWire test methodology provides the lowest risk path for customers to achieve dramatic cost reductions. Using Xilinx FPGA's and HardWire technology provides the customer with a single source for systems, software and silicon. This combination provides the fastest method for prototype development and production of systems based on leading edge programmable logic technology. Each HardWire product family is developed to match the performance and features of specific Xilinx FPGAs. The latest additions to the family of HardWire products are XH3 and XH3L. They are designed to provide significant cost reduction for Xilinx FPGAs including E, EX and XL technology.

Xilinx HardWire Technology Overview

HardWire Products are a family of state-of-the-art sea-of-gates .5µ and .35µ multi-mask ASIC devices. The HardWire product families have been developed to match the performance and features of Xilinx FPGAs.

The HardWire flow is the easiest method for cost reducing an FPGA based system. The Xilinx "Design Once" methodology offers Xilinx customer the advantages of developing prototypes, building pre-production and initial production volumes using Xilinx FPGAs. Once the design is stable and cost reduction is critical; a customer can convert the FPGA to a HardWire device developed especially to match the features and performance of that FPGA.

The HardWire development process is turnkey, and uses few customer engineering resources. It allows production quality HardWire prototypes to be produced in half the time of traditional gate arrays. HardWire devices provide a cost - effective alternative to traditional gate arrays.

Advantages of the Xilinx HardWire Methodology

Converting from an FPGA to a HardWire device has many advantages over standard gate array redesign. The most important advantage is HardWire devices are developed using a fully turnkey process. Customer engineering resources are required to review conversion reports or discuss special features implemented in the FPGA design. No customer engineering resources are required to convert the programmable logic design into a fully tested, completely verified HardWire device. This ease of conversion is available only from Xilinx. HardWire devices are developed using the actual physical database previously created and verified in the process of developing the FPGA design. The HardWire conversion methodology preserves the placement and routing attributes of CLB's used for logic in the original physical database file. If the design is mapped to a third party library at the schematic level for conversion to another technology, the design must be verified and prototyped. Third party implementations will change the placement and routing, thereby changing the design's performance characteristics. This means the new device must be re-verified and re-tested in the system to be certain that the performance and functionality still meet the applications requirements. A comparison of the activities required to convert a HardWire versus a generic gate array is shown in Figure 1.

Re-verifying the Design

In conventional gate array conversion (re-design), the design must be re-verified after the schematic is translated or recaptured. The process of re-verifying a design is rigorous and time consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. A suitable test methodology must be considered and implemented. All this is usually done by the customer, at the customers' expense and risk.

In contrast, no additional customer engineering effort is required when converting to a HardWire device. Customer engineering is involved to discuss features implemented in the FPGA design and review conversion reports. The HardWire design is self-verifying because the actual FPGA database files are used for the conversion. This makes the HardWire conversion process a fully turnkey conversion.

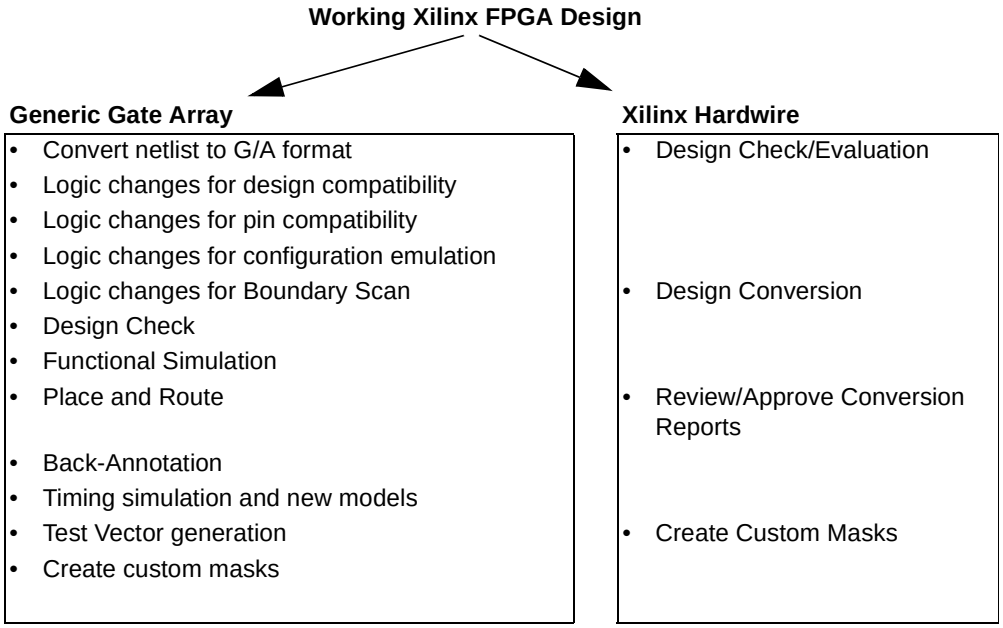

Figure 1: Steps Involved in Converting a PLD Design to a Gate Array as Compared to a HardWire Device

Fault Coverage and Test Vectors

All designs need to be testable. In a traditional gate array, the designer is required to build in testability and generate test vectors to verify chip performance by exercising as much of the device circuitry as possible. Most designers strive for greater than 90% fault coverage. However, they often settle for significantly less because the iterative process is time consuming and increases exponentially as fault coverage is increased. A third party conversion from a Xilinx FPGA to a generic gate array or other similar technology will require test vector generation. Typically, the original designers create test vectors, since they are most familiar with the FPGA's design. This method misuses valuable design resources and reverses the value of the decision to use programmable logic for their ease of design and time-to-market advantage. Another method is to contract with the conversion or gate array vendor to create the test vectors. This method is both expensive and time consuming. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts the liability of determining whether the resulting device is production worthy. In today's competitive market, most projects can not afford the risk of possible re-spins if the design doesn't work.

Converting from a Xilinx FPGA to a HardWire device requires no test vector generation by the customer. HardWire devices use a combination of industry standard and Xilinx patented test generation methods to achieve the most complete fault coverage possible. All HardWire devices are tested using a full scan test methodology.

Packaging and Silicon Considerations

HardWire devices are functionally compatible with Xilinx FPGAs. They are also, whenever possible, physically and mechanically the same. HardWire devices are manufactured in the same fabrication facilities used by Xilinx for the production of FPGA's. This allows a significant reduction in the time and cost associated with qualifying HardWire devices.

Converting from a Xilinx programmable logic device to any third party device means a change in silicon, packaging, assembly and test. Each of these changes adds an element of risk into the qualification process.

Support for the Entire Product Life Cycle

Figure 2 shows the typical life cycle of a high-volume product. It illustrates the optimal way of using the programmable and HardWire devices. During development, prototyping and initial production cycles, the programmable device is the best choice. As the system moves into higher volume production and no additional modifications are being made to the design, a HardWire device can be used in place of the original programmable logic device.

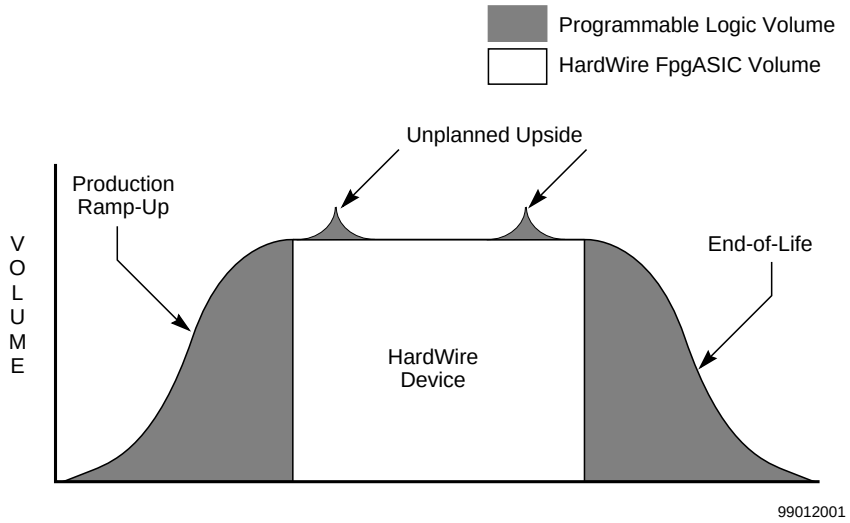

Figure 2: Typical High Volume Product Life Cycle

Since the HardWire device and the programmable logic device are functionally and physically compatible, production can be switched back to the programmable device if the situation warrants. For example, if the demand for the customer's product increases dramatically, production can be increased immediately by fulfilling the additional demand with programmable devices. The change can be made immediately since there is virtually no lead-time for an off-the-shelf programmable device. Production can also be switched to the programmable device as the product ends its life cycle and volume decreases. This eliminates the need for end-of-life buys and the risk of obsolescence.

Furthermore, designs implemented with multiple programmable devices can be cost reduced incrementally, converting one or more of the programmable devices to a HardWire device with the balance remaining as FPGAs. As each FPGA is converted to a HardWire device, the user benefits by having a lower price for that device. This also allows the user to maintain the ease-of-use of off-the-shelf programmable logic in the other sockets. When all of the devices are converted, the storage element (PROM) can be removed, giving even further cost reductions. This flexibility is unique to Xilinx, and allows customers to achieve cost reduction quickly with minimal effort.

HardWire Design/ Production Interface

Figure 3 illustrates how the design, development and production activities for HardWire devices are sequenced in comparison to gate arrays. Using the Xilinx "Design Once" methodology, limited customer activity is needed to develop the HardWire. All HardWire devices are developed using the FPGA actual design database. Using the FPGA design database in conjunction with other documentation supplied by the customer reduces the amount of time required to develop the HardWire device. It allows Xilinx to perform a simple design check procedure prior to generating the HardWire device. The design check along with the customers conversion report review reduces the risk of errors. After the design check is complete the HardWire prototypes can be manufactured. The customer then performs in-system verification of the prototypes. Once this verification is complete the HardWire device can be released to production. Since the functionality of the FPGA and HardWire are compatible, few customer engineering resources are needed to move from the programmable to the HardWire or vice versa. By comparison, using a traditional gate array to reproduce functions implemented in the FPGA would require extensive simulation and test development.

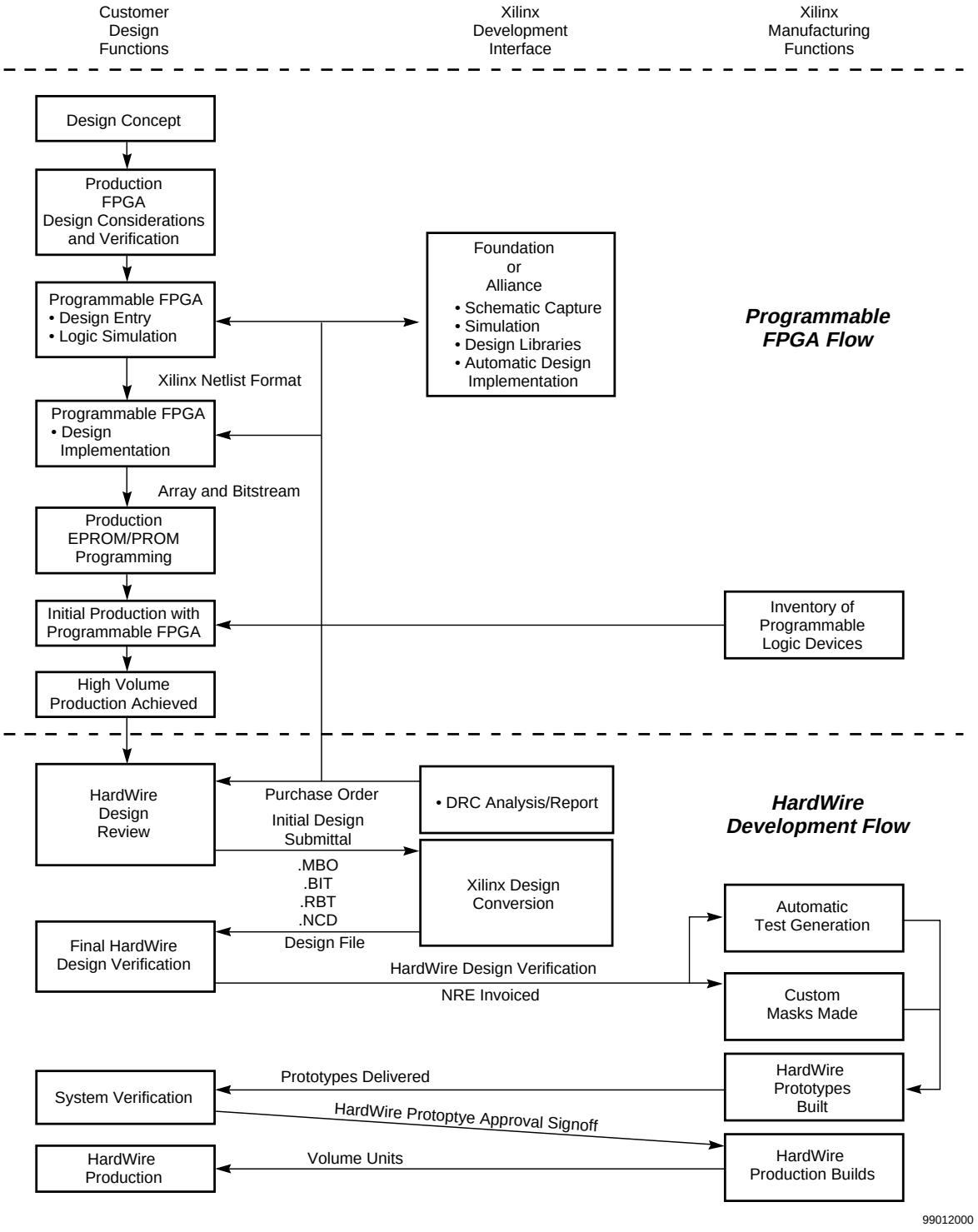

Figure 3: Programmable/HardWire Design/Production Interface

Design Submittal Process

HardWire development time will vary with the addition of features such as RAM, Configuration Emulation and JTAG. Once the complete design submittal kit is received the HardWire conversion will begin. A complete design submittal kit contains the following:

1. Files: A complete list of required files can be found in the HardWire Design Submittal workbook.
2. Hard copy of a board level schematic showing how the FPGA interfaces with other components on the board (if possible).
3. A detailed explanation of any special requirements for the conversion.
4. A design submittal form and NRE PO.

All forms can be found in the HardWire Design Submittal workbook and on the Xilinx web page under HardWire products.

Summary of the Conversion Process

The HardWire conversion process is the simplest way to cost reduce systems designed using FPGAs. The customer is involved in tracking and approving milestones. Xilinx handles the day-to-day activities of converting the design to a HardWire device. Once Xilinx receives a complete design submittal kit the conversion process begins. Xilinx first reviews the design to determine any items that could impact the performance of the HardWire device. A conversion evaluation report is sent to the customer. After the report has been reviewed and the customer is satisfied, conversion begins. At the completion of the conversion the final timing report along with the Design Verification Form (DVF) is sent to the customer. Once the DVF is completed the HardWire files are sent to the mask shop for prototyping. If any custom markings are required they must be submitted to Xilinx with the Design Verification Form (DVF). Prototypes are produced, tested and shipped to the customer for in-system testing. The customer signs the prototype approval form and returns it to Xilinx. Production can begin.

The HardWire Product Families

Each HardWire product family is developed to support the features, density and performance of a specific generation of Xilinx FPGA's. The initial family of HardWire devices (XC23xx, XC33xx and XC43xx) supports XC2xxx, XC3xxx and XC4xxx (no E features) FPGAs. The second generation of HardWire devices (XC5400, XC4400 and XC4400XL) support XC52xx, XC4xxxE, XC4xxxEX and XC4xxxXL FPGAs. These technologies are used to support production requirements only. New designs will be targeted to more current HardWire technology. For new designs developed using Xilinx XC4xxxXL family of FPGAs, the XH3L HardWire family provides the most effective technology, cost and performance. For customers using fast, dense Xilinx XC4xxxE, EX FPGA's the XH3 product family provides the most efficient and cost effective solution available. All HardWire devices support commercial and industrial temperature ranges. See Table 1 for product family details.

Table 1: HardWire Product Families

FPGA Device Family	Speed Grade	Features Supported	HardWire Family	Voltage
XC40xxXL	All	XL	XH3xxL	3.3V
XC40xxEX	All	E, EX	XH3xx	5V
XC40xxXL	All	XL	XC44xxXL	3.3V
XC40xx	All	E, EX	XC44xx	5V
XC52xx	All	All	XC54xx	5V
XC4xxx	All	No E features	XC43xx	5V
XC3xxx	All	All	XC33xx	5V, 3.3V
XC2xxx	All	All	XC23xx	5V, 3.3V

Xilinx HardWire Product Descriptions

XH3 and XH3L Product Descriptions

The XH3 and XH3L HardWire product families were developed to match the performance, density and features of Xilinx XC4xxxE, XC4xxxEX and XC4xxxXL family of FPGA's. These HardWire FpgASIC product families support the features of Xilinx second generation FPGAs. This includes speed grades, Configuration Emulation (CE), JTAG and RAM. The control logic for Configuration Emulation, Power on Reset (POR), Oscillators and full JTAG are built into the XH3 and XH3L base arrays. RAM blocks are incorporated with maximum efficiency. Both XH3 and XH3L use the dense sea-of-gates CMOS CBA technology, from Xilinx partner SiARC, a division of Synopsys. The .5m (XH3) and .35m (XH3L) process geometry used are small enough that die sizes are driven by pad count and not gate count,

except for FPGAs designs with high RAM content. The Xilinx patented DesignLock turnkey conversion methodology is used to develop all XH3 and XH3L devices. XH3 and XH3L provide the most cost-effective method for converting XC4xxxE, XC4xxxEX and XC4xxxXL FPGA's to low cost HardWire FpgASICs.

XH3L Summary

- Features
  - Designed for conversion of XC4xxxXL 3.3v FPGAs.
  - Only used CLB's are mapped.
  - Multiple Masks, state-of-the-art .35µ process technology.
  - On chip scan path test latches.
  - Fully pin for pin compatible with FPGA
  - Smallest possible die size.
- Benefits
  - All Xilinx FPGA features supported, including CE, JTAG and Select RAM.
  - Smallest possible die size used to achieve the lowest possible cost.
  - Technology feature size matched to performance requirements.
  - No customer developed test vectors needed.
  - Drop in replacement for Xilinx FPGAs.

XH3 Summary

- Features
  - Designed for conversion of high density XC4xxxE and EX 5V FPGAs.
  - Xilinx FPGA features built in to the base array.
  - Multiple Masks, state-of-the-art .5µ process technology.
  - Pad counts and gate counts available for the densest FPGA devices.
  - On chip scan path test latches.
  - Fully pin-for-pin compatible with FPGA.
- Benefits
  - All Xilinx FPGA features supported, including CE, JTAG and Select RAM.
  - Patented, turnkey conversion flow.
  - Pads, package and FPGA design content required determine device used.
  - No customer developed test vectors needed.
  - Drop in replacement for Xilinx FPGAs.

HardWire Summary

Xilinx Hardwire products are a family of devices ranging from .5µ to .35µ state-of-the-art sea-of-gates multi-mask ASIC devices. The HardWire flow is the simplest method of cost reduction for FPGA based systems. They are developed using the FPGA's design files. This guarantees the HardWire device will be functionally compatible with the FPGA. No customer generated test vectors are required with HardWire. Each HardWire device is tested using a combination of industry standard and Xilinx patented test methods in a full scan methodology. HardWire prototypes can be developed in half the time of traditional gate array prototypes. HardWire process technologies, conversion methods and testing procedures provide the most cost - effective alternative to traditional gate arrays.