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QPRO™ High-Reliability QML Certified and Radiation Hardened Products for Aerospace and Defense Applications

January 21, 2000 (v2.0)

The High-Reliability Programmable Logic Leader

Xilinx is the leading supplier of High-Reliability programmable logic devices to the aerospace and defense markets. These devices are used in a wide range of applications such as electronic warfare, missile guidance and targeting, RADAR, SONAR, communications, signal processing, avionics and satellites. The Xilinx QPRO family of ceramic and plastic QML products (Qualified Manufacturers Listing), certified to MIL-PRF-38585, provide system designers with advanced programmable logic solutions for next generation designs. The QPRO family also includes select products that are radiation hardened for use in satellite and other space applications.

The Xilinx QPRO family addresses the issues that are critical to the aerospace and defense market:

QML/Best commercial practices. Commercial manufacturing strengths result in more efficient process flows

Performance-based solutions, including cost-effective plastic packages.

Reliability of supply. Controlled mask sets and processes insure the same quality devices, every time, without variation, which remain in production for an extended time.

Off-the-shelf ASIC solutions. Standard devices readily available, no need for custom logic and gate arrays.

Unmatched Product Offering

The QPRO family provides a wide variety of devices, delivering the industry's fastest and biggest devices. The Virtex members of the QPRO family offers FPGAs with densities greater than 1,000,000 system gates, and even larger devices planned for the future. This broad range of devices is available in a wide variety of speed and package options. Both military temperature and full QML/SMD versions are available as standard off-the-shelf products. Select software cores, such as complete PowerPC peripherals, is also available.

Products for Space Applications

Xilinx offers the industry's only radiation hardened reconfigurable FPGAs for satellite and space. These devices are manufactured using an epitaxial wafer process, and have guaranteed total dose, latch up immunity, and low soft upset rates. These products allow for the ultimate in design and mission flexibility in a cost-effective manner.

QML Certification Part of Overall Quality Platform

Being certified to MIL-PRF-38535 QML complemented by ISO-9000 certification results in an overall product quality platform that makes Xilinx a world-class supplier of programmable logic devices. Designers can confidently design with Xilinx for High-Reliability systems with the knowledge they are getting unsurpassed quality and reliability, and long-term commitment to the aerospace and defense market.

Commitment to the Aerospace and Defense Market

Xilinx understands that our customers need to be able to count on their suppliers to be around for the long-term. Xilinx is committed to the long-term support of the aerospace and defense market, and we are continually expanding our product portfolio. Because our focus is in the form of a vertical market concept, we are able to provide emphasis on all of our customer's product requirements.

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Table 1: High Density High Performance and Radiation Hardened Products

Family	Devices	Features
XC/XQ4000/E/EX	XC4005/E XC4010/E XC4013/E XC4025E XQ4028EX	• 5,000-28,000+ gates • Up to 256 user-definable I/Os • Extensive system features include on-chip user RAM, built-in 1149.1 test support and fast carry logic
XQ4000XL	XQ4013XL XQ4036XL XQ4062XL	• Up to 130,000 system gates • 3.3 V, 5V-compatible I/O
XQR4000XL Radiation Hardened	XQR4013XL XQR4036XL XQR4062XL	• Up to 130,000 System Gates • 60K Rads total dose, latchup immune
Virtex	XQV100 XQV300 XQV600 XQV1000	• Up to 1,000,000 System Gates, 2.5V
Virtex Radiation Hardened	XQVR300 XQVR600 XQVR1000	• 100K Rads Total Dose, Latchup Immune

Revision Control

Date	Version	Description
1/98	1.1	Version 1.1 -- High-Reliability and QML Military Products, correct erroneous information page 2 "XC3000 Products", delete last page, table - "Mil-PRF-3853 QML, Xilinx M Grade and Plastic Commercial Flows"
11/98	1.2	Version 1.2 - Added new products, corrected XC3000, XC4000 products.
02/02/00	2.0	Updated Introduction and product listing.

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QPRO Virtex 2.5V QML High-Reliability FPGAs

DS002 (v1.0) October 4, 1999   Preliminary Product Specification

Features

- Certified to MIL-PRF-38535 (Qualified Manufacturer Listing)
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Ceramic and Plastic Packages
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device

- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22 µm 5-layer metal process
- 100% factory tested

Description

The QPRO™ Virtex™ FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the four members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

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Table 1: QPRO Virtex Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQV100	108,904	20x30	2,700	180	40,960	38,400
XQV300	322,970	32x48	6,912	316	65,536	98,304
XQV600	661,111	48x72	15,552	316	98,304	221,184
XQV1000	1,124,022	64x96	27,648	404	131,072	393,216

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QPRO™ Virtex™ 2.5V Radiation Hardened FPGAs

DS028 (v1.0) February 9, 2000   Advance Product Specification

Features

- Radiation hardened FPGAs for space and satellite applications
- Guaranteed total ionizing dose to 100K Rad(si)
- Latch-up immune to LET = 125 MeV cm^2/mg
- SEU immunity achievable with recommended redundancy implementation
- Guaranteed over the full military temperature range ($-55°$C to $+125°$C)
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device

- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22 µm 5-layer epitaxial process

Description

The QPRO Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex radiation hardened family comprises the three members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

Table 1: QPRO Virtex Radiation Hardened Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQVR300	322,970	32x48	6,912	316	65,536	98,304
XQVR600	661,111	48x72	15,552	316	98,304	221,184
XQVR1000	1,124,022	64x96	27,648	404	131,072	393,216

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**QPRO™ XQ4000E/EX
QML High Reliability FPGAs**

May 19, 1998 (Version 2.1)   Product Specification

XQ4000E/EX High-Reliability Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- System featured Field-Programmable Gate Arrays
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XQ4000E/EX output

- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E   -3 for plastic packages only
  -                 -4 for ceramic packages only
  - XQ4028EX -4 for all packages

More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This datasheet contains pinout tables for XQ4010E only. Refer to Xilinx 1998 Databook for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)

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Table 1: XQ4000E/EX Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1024	2560	96	256	PG299, CB228, HQ240, BG352

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

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QPRO™ XQ4000XL Series QML High-Reliability FPGAs

DS029 (v1.2) February 9, 1999

XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
    - XQ4013XL 5962-98513
    - XQ4036XL 5962-98510
    - XQ4062XL 5962-98511
    - XQ4085XL 5962-99575
- For more information contact the Defense Supply Center Columbus (DSCC)
    http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
    - SelectRAM™ memory: on-chip ultra-fast RAM with
        - synchronous write option
        - dual-port RAM option
    - Abundant flip-flops
    - Flexible function generators
    - Dedicated high-speed carry logic
    - Wide edge decoders on each edge
    - Hierarchy of interconnect lines
    - Internal 3-state bus capability
    - Eight global low-skew clock or signal distribution networks
- System Performance beyond 50 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
    - IEEE 1149.1-compatible boundary scan logic support
    - Individually programmable output slew rate
    - Programmable input pull-up or pull-down resistors
    - 12 mA Sink Current Per XQ4000XL Output
- Configured by Loading Binary File
    - Unlimited reprogrammability
- Readback Capability
    - Program verification
    - Internal node observability
- Development System runs on most common computer platforms
    - - Interfaces to popular design environments
    - - Fully automatic mapping, placement and routing
    - - Interactive design editor for design optimization

- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XQ4000E
    - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
    - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- 0.35 μm SRAM process

Introduction

XQ4000X Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated soft-ware to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000X Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

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QPRO™ XQR4000XL Radiation Hardened Field Programmable Gate Arrays

October 5, 1998 (Version 1.0)   Preliminary Product Specification

XQR4000XL Series Features

- Radiation Hardened FPGAs for space and satellite applications
- Guaranteed Total Ionizing Dose
- Latch-up Immune
- Low Soft Upset Rate
- Guaranteed to meet full electrical specifications over –55°C to +125°C
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features

- IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity—over 130,000 usable gates
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- Advanced 0.35μ process
- Processed on Xilinx's QML Line

Table 1: XQR4000X Series Radiation Hardened Field Programmable Gate Arrays

Device	Logic Cells	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-flops	Max. User I/O	Packages
XQR4013XL	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	CB228
XQR4036XL	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	CB228
XQR4062XL	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	CB228

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

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XC1700L Series High Density Serial Configuration PROMs Including XQ1701L QPRO™ Series

July 8, 1999 (Version 2.3)   Product Specification

Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports XC4000EX/XL/XLA/XV fast configuration mode (15.0 MHz)
- Low-power CMOS Floating Gate process
- XC1704L, XC1702L, XC1701L, XQ1701L and the XC17512L are 3.3V devices
- XC1701 is a 5V device only
- Available in compact plastic packages: 8-pin PDIP, 20-pin SOIC, 20-pin PLCC, 44-pin PLCC or 44-pin VQFP.
- QPRO™ parts available in 44-pin ceramic LCC and 20-pin SOIC.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The XC1704L, XC1702L, XC1701L, and the XC17512L are Xilinxs 3.3V series of high density serial configuration PROMs (SPROMs). Included within this family are the XC1701 (5V) and the XQ1701L (3.3V) SPROMs to provide an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmer.
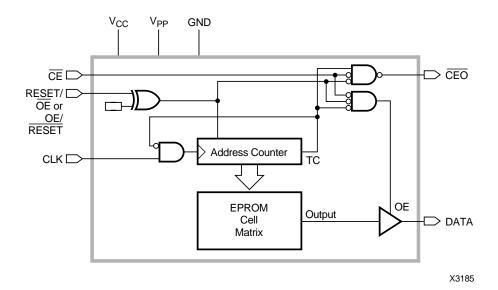

Figure 1: Simplified Block Diagram (does not show programming circuit)