



## **Release Document**

**Foundation Series 2.1i**

**Installation Guide  
and  
Release Notes**

**July 1999**

**Read This Before Installation**

## Foundation Series 2.1i Installation Guide and Release Notes

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5,790,882; 5,795,068; 5,796,269; 5,798,656; 5,801,546; 5,801,547; 5,801,548; 5,811,985; 5,815,004; 5,815,016; 5,815,404; 5,815,405; 5,818,255; 5,818,730; 5,821,772; 5,821,774; 5,825,202; 5,825,662; 5,825,787; 5,828,230; 5,828,231; 5,828,236; 5,828,608; 5,831,448; 5,831,460; 5,831,845; 5,831,907; 5,835,402; 5,838,167; 5,838,901; 5,838,954; 5,841,296; 5,841,867; 5,844,422; 5,844,424; 5,844,829; 5,844,844; 5,847,577; 5,847,579; 5,847,580; 5,847,993; 5,852,323; Re. 34,363, Re. 34,444, and Re. 34,808. Other U.S. and foreign patents pending. Xilinx, Inc. does not represent that devices shown or products described herein are free from patent infringement or from any other third party right. Xilinx, Inc. assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made. Xilinx, Inc. will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

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# Conventions

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This manual uses the following typographical conventions. An example illustrates each convention.

- `Courier font` indicates messages, prompts, and program files that the system displays.

```
speed grade: -100
```

- **Courier bold** indicates literal commands that you enter in a syntactical statement. However, braces “{ }” in Courier bold are not literal and square brackets “[ ]” in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

```
rpt_del_net=
```

**Courier bold** also indicates commands that you select from a menu or buttons that you click in dialog boxes.

```
File → Open
```

```
Click OK
```

- *Italic font* denotes the following items.
  - Variables in a syntax statement for which you must supply values

```
edif2ngd design_name
```

- References to other manuals

See the *Development System Reference Guide* for more information.

- Emphasis in text

If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets “[ ]” indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

`edif2ngd [option_name] design_name`

- Braces “{ }” enclose a list of items from which you must choose one or more.

`lowpwr = {on | off}`

- A vertical bar “|” separates items in a list of choices.

`lowpwr = {on | off}`

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'  
IOB #2: Name = CLKIN'  
.  
.  
.
```

- A horizontal ellipsis “. . .” indicates that an item can be repeated one or more times.

`allow block block_name loc1 loc2 . . . locn;`

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## Introduction

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The Xilinx Foundation Series provides a complete, front-to-back environment for the design of Xilinx programmable logic devices. This manual explains how to install the PC-based Xilinx Foundation Series software products listed below.

- **Base (DS-FND-BAS-PC)**  
Supports only the smaller Xilinx FPGA and CPLD devices. The FPGA and CPLD device tables in the “Device and Package Support” chapter identify which devices are supported by the Base software product. This product does *not* include Express VHDL or Verilog HDL capabilities.
- **Base Express (DS-FND-BSX-PC)**  
Supports the same devices as Base, but includes Express HDL synthesis and optimization capabilities. (The Express Constraints Editor and Time Tracker GUIs to enter constraints and analyze timing prior to design implementation are *not* included. The Express Schematic Viewer GUI is also *not* included.)
- **Standard (DS-FND-STD-PC)**  
Supports all FPGA and CPLD devices. This product does *not* include Express VHDL or Verilog HDL capabilities.
- **Foundation Express (DS-FND-EXP-PC)**  
Supports the same devices as Standard, but includes complete FPGA Express capabilities. This encompasses HDL synthesis and optimization capabilities plus Express Constraints Editor and Time Tracker GUIs to enter constraints and analyze timing prior to design implementation that are not included with Base Express. This product also includes the Express Schematic Viewer, which enables viewing of the RTL and optimized schematic representations of your HDL.

## Installation Procedure Guidelines

The following is a summary of the steps to follow for getting ready to use your software.

1. Read this release document.

Make sure to check the “System Requirements” chapter for operating and disk space requirements.

2. Install your Foundation design environment software.

Follow the instructions in the “Typical Installation” chapter.

You may need to reboot your PC to allow the new/modified environment variables and path statement to take effect. The setup program will inform you if you need to reboot.

3. Register your software with Xilinx

In order to receive FREE future updates and product information, you need to register your software with Xilinx. You can register online at the end of the installation. Or, you can fax or mail the enclosed registration card to Xilinx.

4. Install the Foundation online books and index (optional).

The Foundation Series 2.1i books to accompany the 2.1i design environment are available in HTML and Adobe Acrobat PDF formats. They can be read from the web at <http://support.xilinx.com> or from the Documentation CD. Or, they can be installed on your PC. Enhanced searching capability is available with the provided Docsan documentation index.

Follow the instructions in the “Documentation” chapter for accessing and installing the books and the documentation index.

5. Begin creating designs.

See the “Getting Started” chapter for basic information on starting and using the Foundation software and the online documentation index. A Foundation multimedia quick start demo (run from the Documentation CD or Design Environment CD) is also available to get you started.

## 6. License your Express software.

Licensing is required for Base Express and Foundation Express only. You do *not* need to license the Base or Standard products.

After installing Base Express or Foundation Express software, a temporary, evaluation license is activated for you automatically if you do not already have a license.dat file or SET\_LM\_LICENSE variable defined.

For Base Express, the temporary license has the following limitation:

- No bitstream can be created for downloading.

For Foundation Express, the temporary license has the following two limitations:

- The Express Constraints Editor, Time Tracker, and Schematic Viewer GUIs are not available.
- No bitstream can be created for downloading.

Please authorize your Express software within 90 days to receive a full-function Express license to gain full Base Express 2.1i or Foundation Express 2.1i functionality. Refer to the “Express Software Licensing” chapter. Also refer to the License and Registration Instructions located in your package.

If you experience problems with the installation, operation, or verification of your installation, online technical support is available 24 hours a day, 7 days a week at <http://support.xilinx.com>. If you need additional support, contact the Xilinx Technical Support Hotline. The Hotline numbers and hours are shown in the “Software Service and Support” chapter.

## Contents of this Release

The Foundation Series 2.1i software consists of three CDs:

- **Foundation Series 2.1i Design Environment CD**

This CD includes the Xilinx CORE Generator, userware samples/tutorial files, and the multimedia quick start demo in addition to the design environment software. It also contains installation programs for Netscape Navigator 4.5 and Adobe Acrobat Reader 3.01.

- **Foundation Series 2.1i Documentation CD**

In addition to HTML browser readable online books, this CD includes the Docsan documentation index, printable Adobe Acrobat PDF versions of the books, the multimedia quick start demo, and installers for Netscape Navigator 4.5 and Adobe Acrobat Reader 3.01.

- **Model Technology (MTI) ModelSim™ Evaluation CD**

ModelSim is an HDL behavioral simulator from MTI for VHDL and Verilog. It includes its own installation instructions. Sale and support of this product are handled by MTI.

## Versions and Compatibility

The Foundation 2.1i product consists of the following software systems:

Vendor	Description	Vendor Version
Aldec®	Design Entry Tools	3.1
Synopsys®	Base Express *	3.2
Synopsys®	Foundation Express *	3.2
DataI/O®	ABEL HDL Design Entry Tools	6.3
Xilinx®	Design Implementation Tools	2.1i
Sidana Systems, Inc.	Docsan™ Documentation Index	3.0.1
Globetrotter	FLEXlm™ security for Express	6.1

\* Base Express and Foundation Express are optional packages

## New Features in Foundation 2.1i

Following is a list of the major new features supported for this release. Refer to the *What's New in Foundation 2.1i* online help file for more information on the new features.

- New version (v3.2) of Foundation Express
- CORE Generator™ tool integration
- Xilinx Constraints Editor integration



- Enhancements to the Archiving projects feature
- Implementation guide file support
- Virtex support in the Floorplanner
- CPLD ChipViewer
- FPGA Editor
- MultiLINX cable support in the Hardware Debugger
- Redesigned Implementation option dialogs
- Online books available in HTML and PDF formats
- Docsan viewer/index for online books
- Direct link to Xilinx Customer Service and Support and Online Documentation web site from Project Manager Help

You can access Xilinx web sites directly from the Project Manager. Select **Help** → **Online Documentation** for online software manuals or **Help** → **Xilinx on the Web** to access the Xilinx Customer Service and Support web site. This site contains links to Answers Search, Software Updates, Expert Journals, Application Notes and more.

## Items Not Supported In This Software Release

- The netlist output program NGD2XNF is no longer supported.
- LogiBLOX does not support Virtex devices.
- The Hardware Debugger supports the USB port only on the Windows98 operating system. It does not support this port on other operating systems.
- Virtex guaranteed pin-to-pin timing is available only through updated speed files. The speed files will be available on the <http://support.xilinx.com> web site.



## Device and Package Support

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This chapter identifies the Xilinx FPGA and CPLD devices supported in this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*. *The Programmable Logic Data Book* is available in hard copy and on the Xilinx web site (<http://support.xilinx.com>).

### Xilinx FPGA Devices

The following is a master table of Xilinx FPGA devices for this release. An “X” in the Base Software Device column indicates that the device is available in the Base and Base Express software products. All devices are available in the Standard and Foundation Express software products.

Device	Packages	Base Software Device <sup>a</sup>
<b>Spartan Family:</b>		
XCS05	PC84, VQ100	X
XCS10	PC84, VQ100, TQ144	X
XCS20	PQ208, VQ100, TQ144	X
XCS30	PQ208, VQ100, TQ144, PQ240, BG256	X
XCS40	PQ208, PQ240, BG256	X
<b>SpartanXL Family:</b>		
XCS05XL	PC84, VQ100	X
XCS10XL	PC84, VQ100, TQ144	X
XCS20XL	PQ208, VQ100, TQ144	X
XCS30XL	PQ208, VQ100, TQ144, PQ240, BG256	X
XCS40XL	PQ208, PQ240, BG256	X

Device	Packages	Base Software Device <sup>a</sup>
<b>Virtex Family:</b>		
XCV50	BG256, CS144, FG256, PQ240, TQ144	X
XCV100	BG256, CS144, FG256, PQ240, TQ144	
XCV150	BG256, BG352, FG256, FG456, PQ240	
XCV200	BG256, BG352, FG256, FG456, PQ240	
XCV300	BG352, BG432, FG456, PQ240	
XCV400	BG432, BG560, FG676, HQ240	
XCV600	BG432, BG560, FG676, FG680, HQ240	
XCV800	BG432, BG560, FG676, FG680, HQ240	
XCV1000	BG560, FG680	
<b>XC4000E Family:</b>		
XC4003E	PC84, PQ100, VQ100, PG120	X
XC4005E	PC84, PG156, PQ100, PQ160, PQ208, TQ144, CB164	X
XC4006E	PC84, TQ144, PG156, PQ160, PQ208	X
XC4008E	PC84, PQ160, PG191, PQ208	X
XC4010E	PC84, PQ160, PG191, PQ208, HQ208, BG225, CB196	
XC4013E	PQ160, PQ208, HQ208, PG223, BG225, PQ240, HQ240, CB228	
XC4020E	PG223, HQ208, HQ240	
XC4025E	PG223, HQ240, PG299, HQ304, CB228	
<b>XC4000EX Family:</b>		
XC4028EX	BG352, CB228, HQ208, HQ240, HQ304, PG299	
XC4036EX	HQ304, BG432, PG411, BG352, HQ240	
<b>XC4000L Family:</b>		
XC4005L	PC84, PQ100, PQ208	X
XC4010L	PC84, TQ176, PQ208	X
XC4013L	PQ208, BG225, PQ240	X

Device	Packages	Base Software Device <sup>a</sup>
<b>XC4000XL Family:</b>		
XC4002XL	PC84, PQ100, VQ100	X
XC4005XL	PC84, PQ100, PQ160, PQ208, TQ144, VQ100	X
XC4010XL	BG256, PC84, PQ100, PQ160, PQ208, TQ144, TQ176	X
XC4013XL	BG256, CB228, HT144, HT176, PG223, PQ160, PQ208, PQ240	X
XC4020XL	BG256, HT144, HT176, PQ160, PQ208, PQ240	
XC4028XL	BG256, BG352, HQ160, HQ208, HQ240, HQ304, PG299	
XC4036XL	BG352, BG432, CB228, HQ160, HQ208, HQ240, HQ304, PG411	
XC4044XL	BG352, BG432, HQ160, HQ208, HQ240, HQ304, PG411	
XC4052XL	BG560, BG432, HQ240, HQ304, PG411	
XC4062XL	BG432, CB228, HQ240, HQ304, BG560, PG475	
XC4085XL	BG432, BG560, PG559	
<b>XC4000XLA Family:</b>		
XC4013XLA	BG256, PQ160, PQ208, PQ240	
XC4020XLA	BG256, PQ160, PQ208, PQ240	
XC4028XLA	BG256, BG352, HQ160, HQ208, HQ240	
XC4036XLA	BG352, BG432, CB228, HQ160, HQ208, HQ240	
XC4044XLA	BG352, BG432, HQ160, HQ208, HQ240, HQ304	
XC4052XLA	BG352, BG432, BG560, HQ160, HQ208, HQ240, HQ304	

Device	Packages	Base Software Device <sup>a</sup>
XC4062XLA	BG352, BG432, BG560, CB228, HQ160, HQ208, HQ240, HQ304	
XC4085XLA	BG352, BG432, BG560, HQ160, HQ208, HQ240, HQ304	
<b>XC4000XV Family:</b>		
XC40110XV	BG352, BG432, BG560, HQ240	
XC40150XV	BG352, BG432, BG560, HQ240, PG559	
XC40200XV	BG432, BG560	
XC40250XV	BG432, BG560, PG559	
<b>XC3000A Family:</b>		
XC3020A	CB100, PC68, PC84, PG84, PQ100	X
XC3030A	PC44, VQ64, PC68, PC84, PG84, PQ100, VQ100	X
XC3042A	PC84, PG84, PP132, PG132, CB100, PQ100, VQ100, TQ144	X
XC3064A	PC84, PP132, PG132, TQ144, PQ160	X
XC3090A	PC84, PQ160, TQ144, CB164, PP175, PG175, TQ176, PQ208	X
<b>XC3000L Family:</b>		
XC3020L	PC84	X
XC3030L	VQ64, PC84, VQ100	X
XC3042L	PC84, VQ100, TQ144	X
XC3064L	PC84, TQ144	X
XC3090L	PC84, TQ144, TQ176	X
<b>XC3100A Family:</b>		
XC3120A	PC68, PC84, PG84, PQ100, CB100	X
XC3130A	PC44, PC68, PC84, PG84, PQ100, VQ100, VQ64	X
XC3142A	PC84, PG84, PP132, PG132, CB100, PQ100, VQ100, TQ144	X
XC3164A	PC84, PP132, PG132, PQ160, TQ144	X

Device	Packages	Base Software Device <sup>a</sup>
XC3190A	PC84, PQ160, TQ144, CB164, PP175, PG175, TQ176, PQ208	X
XC3195A	PC84, PQ160, CB164, PP175, PG175, PQ208, PG223	X
<b>XC3100L Family:</b>		
XC3142L	PC84, VQ100, TQ144	X
XC3190L	PC84, TQ144, TQ176	X
<b>XC5200 Family:</b>		
XC5202	VQ64, PC84, PG156, PQ100, TQ144, VQ100	X
XC5204	PC84, PG156, PQ100, PQ160, TQ144, VQ100	X
XC5206	PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100, TQ176	X
XC5210	PC84, PG223, BG225, PQ160, PQ208, PQ240, TQ144, TQ176	X
XC5215	BG225, BG352, HQ304, HQ208, HQ240, PQ160, PG299	X

a. Base Devices are supported in the Base and Base Express software products. The Standard and Foundation Express software products support all devices.

## Xilinx CPLD Devices

The following is a master table of Xilinx CPLD devices for this release. An “X” in the Base Software Device column indicates that the device is available in the Base and Base Express software products.

**Note:** All CPLD devices are available in the Base, Base Express, Standard, and Foundation Express software products.

Device	Packages	Base Software Device <sup>a</sup>
<b>XC9500 Family:</b>		
XC9536	PC44, VQ44, CS48	X
XC9572	PC44, PC84, PQ100, TQ100	X
XC95108	PC84, PQ100, TQ100, PQ160	X
XC95144	PQ100, PQ160, TQ100	X
XC95216	HQ208, PQ160, BG352	X
XC95288	HQ208, BG352	X
<b>XC9500XL Family:</b>		
XC9536XL <sup>b</sup>	CS48, PC44, VQ64	X
XC9572XL <sup>b</sup>	CS48, PC44, TQ100, VQ64	X
XC95144XL <sup>b</sup>	CS144, TQ100, TQ144	X
XC95288XL <sup>b</sup>	BG256, CS280, PQ208, TQ144	X
<b>XC9500XV Family:</b>		
XC9536XV <sup>b</sup>	CS48, PC44, VQ64	X
XC9572XV <sup>b</sup>	CS48, PC44, TQ100, VQ64	X
XC95144XV <sup>b</sup>	CS144, TQ100, TQ144	X
XC95288XV <sup>b</sup>	BG256, CS280, PQ208, TQ144	X

a. Base Devices are supported in the Base and Base Express software products. The Standard and Foundation Express software products support all devices.

b. Not yet supported for JEDEC map creation.



## High-Reliability Military and Aerospace XQ Devices

Please see *The Programmable Logic Data Book* for available Mil/Aero device, packages, and speed grade options. The speed grades listed in the High-Reliability and QML Military Products section of the data book are guaranteed over the specified military temperature operating range. You may then use the generic device type and speed grade in the development system software accordingly.

For production ordering purposes, please note that Xilinx new QML products are designated with a special "XQ" prefix, e.g., XQ4036XL-3CB228M. This indicates devices manufactured to the MIL-PRF-38535 (QML) process flow. Standard Microcircuit Drawing (SMD) part numbers controlled by DSCC can be ordered as well.

## Virtex Devices and Support

The Virtex family supports the EDIF netlist input format. Virtex does not support XNF for back-annotation. Design download is supported through the Hardware Debugger software. Readback is supported through the JTAG Programmer software.

LogiBLOX is not supported for Virtex devices.

Virtex guaranteed pin-to-pin timing is available only through updated speed files. These speed files will be posted to the [support.xilinx.com](http://support.xilinx.com) web site.



## System Requirements

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Ensure the optimum use and operation of your new design tools by installing Foundation Series 2.1i on the recommended hardware with sufficient memory (RAM and swap).

### PC Basics

The following list specifies the type of PC you should have to create Foundation designs for Xilinx FPGA or CPLD devices.

- IBM PC or compatible PC with a Pentium<sup>®</sup> processor, 120 MHz clock speed or greater, 2 GB disk space or greater recommended.
- System memory (RAM)—32 MB to 64 MB (dependent on device)
- Swap space—48 MB to 128 MB (dependent on the Xilinx devices you use)
- Windows 95<sup>®</sup>, Windows 98<sup>®</sup>, or Windows NT 4.0<sup>®</sup> (with Service Pack 3 or 4 installed)
- SVGA 17" monitor
- Keyboard
- Mouse—2-button or 3-button (Microsoft Windows compatible). On a 3-button mouse, the middle button is not used.
- 4x CD-ROM drive
- Ports—Two ports (one for a pointing device and one parallel port for the parallel download cable, if needed). You can share the parallel port used for the parallel download cable.

## Disk Space

The disk space required for typical installations is dependent on the software tools, devices, online books, and tutorials/samples you choose to install. You need to have some idea of the Xilinx devices you want to target for your designs. To conserve disk space, install a minimum number of devices. You can always use the Installation program again later to add more devices, if necessary.

**Warning:** The disk space numbers given in this book and on the installation screens represent the total number of bytes to be delivered for installation of that tool/device. The actual disk space used depends on your PC's file system. For example, if you are using a machine with FAT 16-type file partitioning, the unzipped files may take up as much as 10 times more disk space than indicated.

**Table 3-1 Disk Space for a Typical Installation of the Design Environment**

Configuration	All Options/Devices <sup>a</sup>
Base	389.0 MB
Base Express	461.4 MB
Standard	791.8 MB
Foundation Express	864.2 MB

a.No online books are included in these numbers. You can reduce these numbers by selecting only the devices you plan on using.

Refer to the “Typical Installation” chapter for information on the disk space required to install each component and device.

The PC Lab Installation includes only the Xilinx device download tools: JTAG Programmer, Hardware Debugger, and PROM File Formatter.

**Table 3-2 Disk Space for a PC Lab Installation**

	Disk Space
Xilinx Device Download Tools	7.5 MB

The disk space required for the Documentation CD contents is shown in the following table. This includes the documentation index and all available HTML online books.

**Table 3-3 Disk Space for HTML Books and Index**

	Disk Space
All HTML books and index	37.0 MB

## System Memory (RAM) and Swap Space

The various steps for designing Xilinx FPGAs or CPLDs require a substantial amount of memory, as shown in the following table.

**Table 3-4 Memory Requirements**

Xilinx Packages	RAM	Virtual Memory (Swap Space)
Base or Base Express	48 MB	64 MB
Standard or Foundation Express	64 MB	128 MB

The preceding table indicates the system requirements for a typical design; however, the unique characteristics of each individual design affects the actual system resources required. Each designer should use memory, processor, and disk monitoring utilities to get an understanding of the exact resources being utilized during each stage of the design cycle. The operating system adds additional memory overhead, as do any active applications. Some designs can be implemented using less than the specified memory while other complicated or large designs may require additional memory. Each designer should monitor the system resources being utilized and adjust the resources if necessary.

Swap file size requirements also vary with the design and constraint set size. By default, Windows 95/98 manages its swap file size automatically, but for Windows NT, you may need to increase it. Typically, your Windows NT swap file size should be twice as large as your system RAM amount.

It is important to note that slower machines, or machines with less than the recommended RAM and/or swap space, will exhibit longer runtimes.

## Recommendations for XC4000EX/XL/XV/XLA Designs

Due to the size and complexity of the XC4000EX/XL/XV/XLA devices, Xilinx recommends that designs for those devices be compiled using a high-performance computer. 64MB of RAM as well as 64MB of swap space is required to compile designs for those devices. However, Xilinx recommends that 128MB of both RAM and swap space be used. For the very large XC40200XV and XC40250XV devices, 256 MB is recommended.

## Recommendations for Virtex Designs

Due to the size and complexity of the Virtex devices, Xilinx recommends that Virtex designs be compiled using a high-performance computer. 64MB of RAM as well as 64MB of swap space is required to compile Virtex designs. However, Xilinx recommends that 256 MB of both RAM and swap space be used. For the very large Virtex devices (XCV800 and XCV1000), 512 MB is recommended.

## Directory Permissions

Write permissions must exist for all directories containing design files to be edited.

## Typical Installation

---

This chapter describes a typical installation of the Foundation Design Environment software.

Before beginning, ensure that your system meets the requirements described in the “System Requirements” chapter.

After you install the Base Express or Foundation Express product, be sure to register and authorize your software within 90 days to obtain full Base Express 2.1i and Foundation Express 2.1i functionality. Refer to the “Express Software Licensing” chapter for details.

**Note:** If you are upgrading from a previous version of Foundation, please read the “Upgrading to Foundation 2.1i” chapter before proceeding with any installation.

## Prerequisites

Some basic information that you need to do a Typical Installation of the software is described in the following subsections.

### CD Key

You are required to enter your name, company, serial number, and CD key in the User Information screen before you can complete a typical installation. A sticker with your product CD Key is located on the back of your Design Environment CD case. The CD Key has the format *XXXXnnnnnnnn* where *X* is an alphabetic character and *n* is a numeric character.

### Serial Number

Your customer serial number (SN) identifies you for Xilinx Customer Support. For existing customers, the serial number is on the outside

of the box (on the shipping label) the upgrade was shipped in. New customers will find their new serial number on a sticker on the back of the Design Environment CD case as well as on the shipping box.

**Note:** If you cannot find your serial number, type `xilinx` in the Serial Number field.

## IBM Anti-Virus Program

The IBM anti-virus program does not let the installer create a Xilinx folder. If you have this program installed, remove it before beginning the installation.

## File Permissions

The permissions for the ALDEC.LOG and ALDEC.INI file must be set for read/write access. If your WINNT directory is set for read only, then the BTL.INI file must be modified; set the TRNFILE setting to a directory that has read/write access.

## System Registry/Autoexec.bat

During installation of the design entry tools, changes are made to the System Registry in Windows 95/98/NT. You can choose whether you want to have the install program set up the XILINX and PATH variables. For Windows NT, these variables are set up in the Registry. For Windows 95/98, these variables are set up in the autoexec.bat file.

**Note:** If you have a dual boot system (that is, you can boot either Windows 95/98 or Windows NT), registry changes are made only for the Window system from which you are installing the Xilinx software.

You must have System Administrator permissions to make changes to the Windows NT Registry when you install the software.

## Licensing for Express

The LM\_LICENSE\_FILE environment variable is used by the FLEXlm software to enable various components of the Base Express and Foundation Express products. The installation program defines the variable for the temporary evaluation license to be `c:\fndtn\data\license.dat`. Refer to the “Express Software Licensing” chapter for more details.



## Using ABEL

If you are using ABEL (or XABEL), the entire Foundation software package must be installed on your local PC's hard drive. The ABEL compiler does not run reliably over a network.

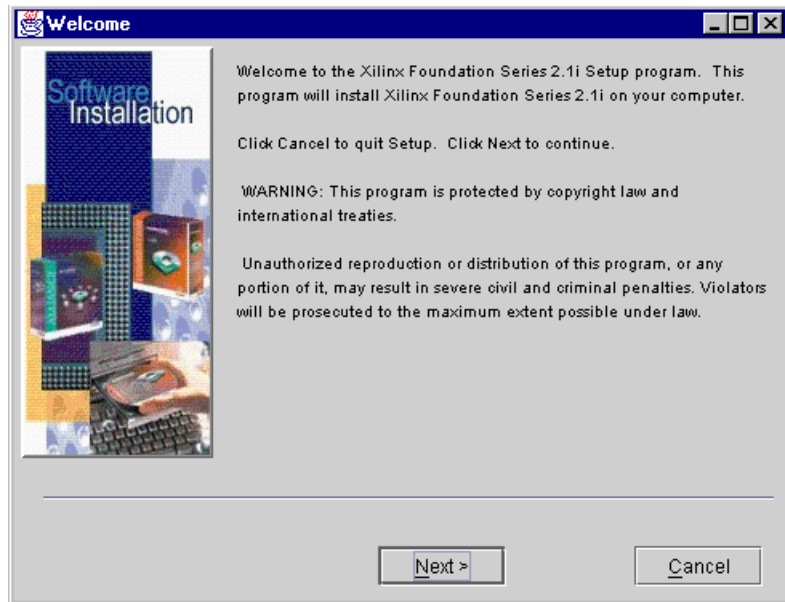
## Start the Installation

To start the installation, insert the Foundation Series 2.1i Design Environment CD into the CD-ROM drive.

If your system has the Auto Run feature enabled, the Foundation installer starts automatically.

If you do not have the Auto Run enabled on your system, select **Start** → **Run**. Type **d:\setup.exe** in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the "d" drive, substitute the appropriate drive designation.)

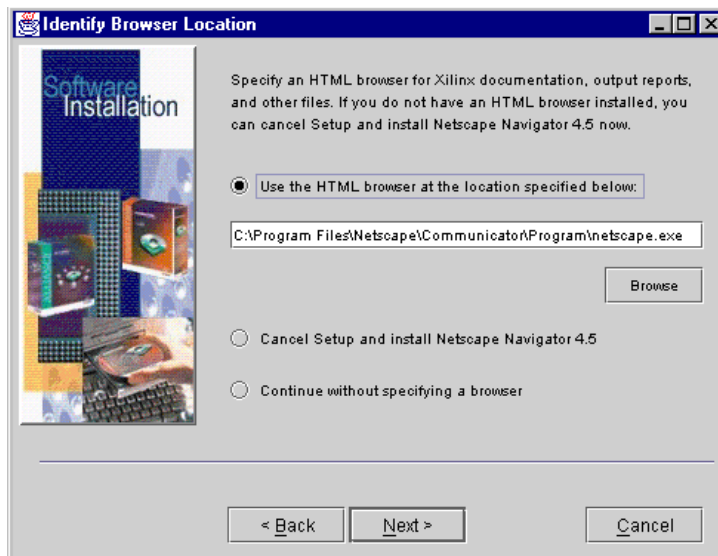
The first screen is the Welcome Screen. Click **Next** when you are ready to proceed with the installation.



## Identify Browser Location

You need to use a Java-enabled HTML browser, such as Netscape Navigator 4.5 or Internet Explorer 4.0, to view the Xilinx online book collection, some implementation output reports, and other related documentation.

Select one of the displayed options and then click **Next** to continue.



### Use a Currently Installed Browser

To use a browser that is already installed on your PC, click the **Use the HTML browser at the location specified below** option. If the desired browser location is not already displayed, type the path or click the **Browse** button to locate the browser you want to use.

### Install Netscape Navigator 4.5

If you would like to install Netscape Navigator, click the **Cancel Setup and Install Netscape Navigator 4.5** option. If you select this option, the Foundation Design Environment installation halts when you click **Next**. The Netscape installation program is initiated automatically. Follow the instructions on the Netscape installation screens to proceed. After you finish installing Netscape

Navigator, you can restart the Foundation Series 2.1i Design Environment installation by selecting `setup.exe` from the CD.

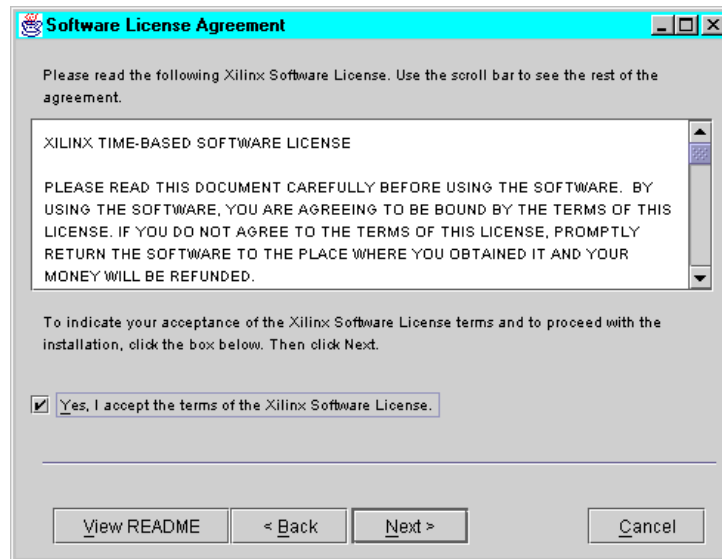
## Continue without Specifying a Browser

If your PC does not have an HTML browser and you do not want to install one now, you can opt to continue with the Foundation Series 2.1i Design Environment installation and install a browser later. You will not be able to view the Xilinx online book collection and certain online reports without an HTML browser.

## Read Software License Agreement

The installation program displays the Xilinx licensing agreement. Read the agreement.

**Note:** The Xilinx software license agreement is a “time-based” (one-year) software license. Please read the license agreement to become familiar with its terms.



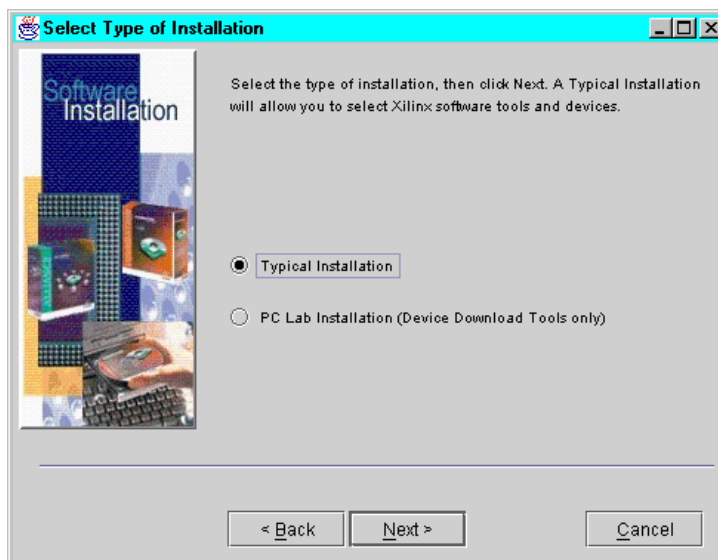
To view the contents of the README.txt file for this release, click the **Display README** button. A new window opens to display this file. This window remains open until you choose to close it by clicking **OK** at the bottom of the README window.

You must indicate your acceptance of the license agreement by clicking the “Yes” box at the bottom of the screen. The box must be checked before you can click **Next** to continue with the installation.

## Select Type of Installation

When the Type of Install screen appears, select **Typical Installation**. A typical installation allows you to select Foundation software design entry tools, implementation tools, Xilinx implementation devices, sample designs, and other components.

Refer to the “PC Lab Installation” chapter for complete information on that option.



## Enter User Information

After you select a Typical Installation and click **Next**, the User Information screen appears.

You *must* enter your name, company name, serial number, and CD key in the User Information screen to progress to the next screen. The CD key is located on a sticker on the back of your Design Environment CD case.

Enter your customer serial number here also to identify you for Xilinx customer support. The serial number is located on the shipping box. It is the number preceded by “SN:”. For new customers, it is also on the back of the CD case along with the product CD Key.

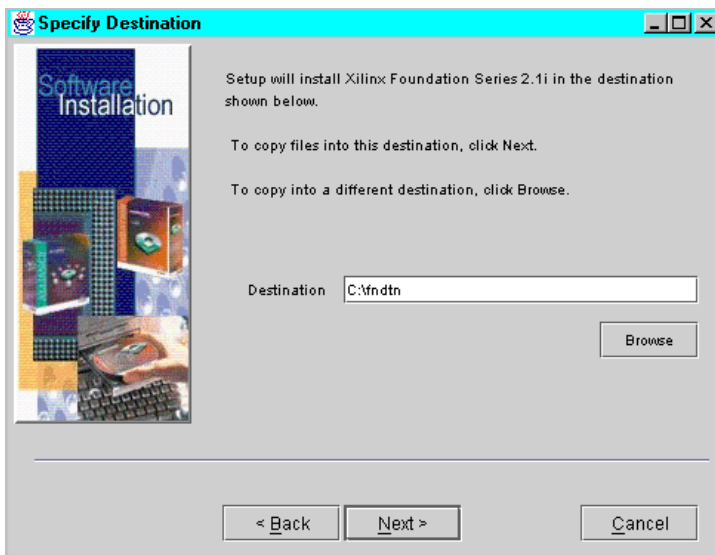
**Note:** If you cannot find your serial number enter **xilinx** in the Serial Number field.

## Specify Destination

When the Specify Destination screen appears, you can install the product in the default folder c:\Fndtn or choose another folder. Click **Browse** to choose another folder, if needed.

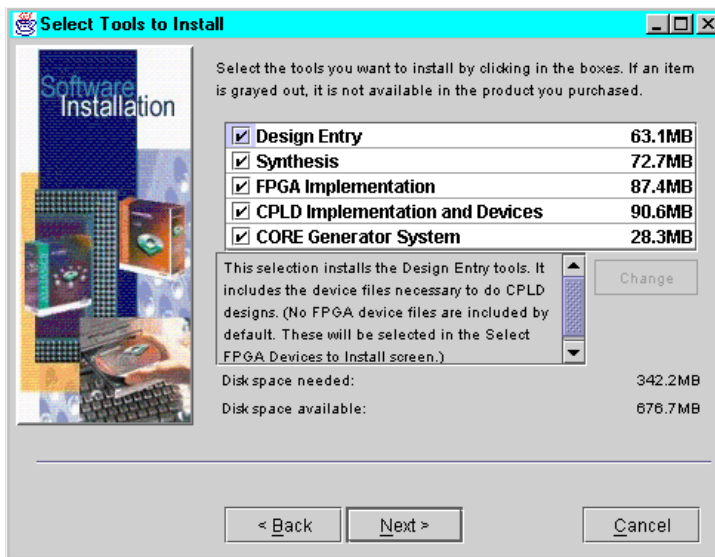
Click **Next** when the desired Destination Folder is selected.

The program displays a “new directory creation” confirmation message if you specified a directory that does not currently exist.



## Select Tools to Install

In the Select Tools to Install screen, click the box to the left of the tool to select it for installation. No tools are selected by default.



Installations of (non-Express) Base and Standard products do not include the Synthesis component. Therefore, it is grayed out in the list for those configurations.

To view a description of a tool, click on the tool name.

**Warning:** The numbers after each item indicate the total number of bytes to be delivered for installation of that tool. The actual disk space used depends on your PC's file system. If you are using a machine with FAT 16-type file partitioning, the unzipped files may take up more space (as much as 10 times more) than indicated.

## Design Entry Tools

Select this item to install the program executables and device libraries necessary for Foundation's schematic design entry, HDL design entry, and Finite State Machine entry.

This selection automatically installs all the device libraries necessary to enter designs for XC9500, XC9500XL, and XC9500XV CPLD devices.

To have FPGA device libraries installed for design entry, you will need to select the FPGA devices you intend to target in the "Select FPGA Devices" screen.

## Synthesis Tools

The Synthesis Tools options is available only if you are installing the Base Express or Foundation Express products.

Select this item to install all the synthesis executables, common library files, and Xilinx macro files used for Foundation HDL synthesis.

This selection automatically installs all the device libraries necessary to synthesize XC9500, XC9500XL, and XC9500XV CPLD designs.

To have FPGA synthesis libraries installed, you will need to select the FPGA devices you want to target in the "Select FPGA Devices" screen.

For the Foundation Express product only, the option also installs the Express Constraints Editor and Timing Analyzer.

## FPGA Implementation Tools

Select this component to install all the FPGA implementation programs (Translation, Map, Place and Route, etc.) used by Foundation's Flow Engine to implement a design in an FPGA.

If you select this option, you must select the FPGA devices you want to target from the Select FPGA Devices to Install screen to have the appropriate device files installed for design implementation on those devices.

This selection also installs all the Xilinx device download tools (JTAG Programmer, Hardware Debugger, and PROM File Formatter) and the ABEL Interface.

## CPLD Implementation Tools and Devices

Select this component to install the following tools:

- All the CPLD implementation programs (Translation, the Fitter, etc.) used by the Flow Engine to implement a design in a CPLD device
- All the device download tools (JTAG Programmer, Hardware Debugger, and PROM File Formatter)
- The ABEL Interface
- All device files necessary for CPLD implementation. The CPLD device families and the included devices for this release are as follows:
  - XC9500 device family  
XC9536, XC9572, XC95108, XC95144, XC95216, XC95288
  - XC9500XL device family  
XC9536XL, XC9572XL, XC95144XL, XC95288XL
  - XC9500XV device family  
XC9536XV, XC9572XV, XC95144XV, XC95288XV

## CORE Generator System

Select this component to install the CORE Generator System. The Xilinx CORE Generator system is an easy to use design tool that

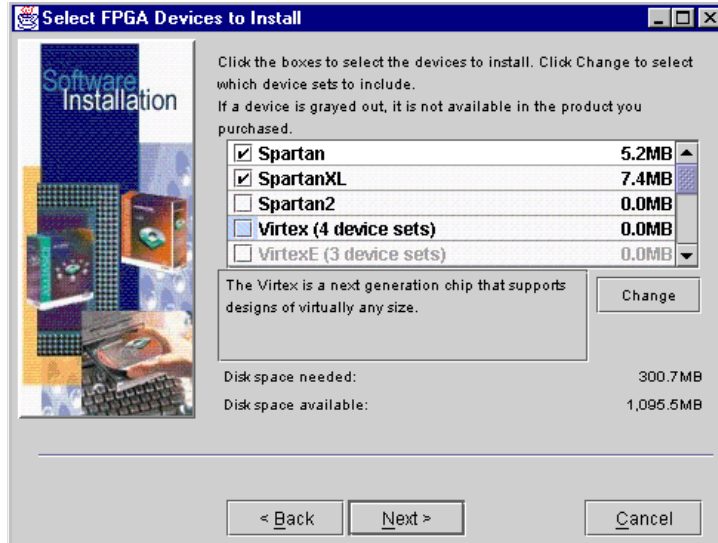


delivers parameterizable cores, optimized for Xilinx FPGAs. The CORE Generator library includes cores as complex as DSP filters and multipliers, and as simple as delay elements. You can use these cores as building blocks in order to complete your designs more quickly. The cores have been completely tested for compatibility with Foundation 2.1i software.

The CORE Generator data sheets and other documentation require the Adobe Acrobat Reader. If the Acrobat Reader is not already installed on your system, you will be given the opportunity to install it after the Foundation installation completes. Or, you can access the `DocTools/Acrobat/english` directory on the Design Environment CD and double click on `ar32e301.exe` to start the Acrobat Reader installation program.

## Select FPGA Devices to Install

The Select FPGA Devices to Install screen appears after the Select Tools screen if you selected Design Entry, Synthesis, or FPGA Implementation tools. For these tools, you must also select the FPGA devices, if any, that you intend to target for your designs.



No devices are selected by default. If a device is grayed out on this screen, it is not available in the product you purchased.

**Note:** If you intend to target CPLD devices only, you need not select any FPGA devices at this screen.

If you purchased the Standard or Foundation Express package, all Xilinx devices (except for Spartan2 and VirtexE) are available. If you purchased a Base or Base Express package, you can select the smaller devices only; the larger devices are grayed out. The FPGA device table in the “Device and Package Support” chapter identifies the Base software devices.

**Warning:** The numbers in parentheses after each device family indicate the total number of bytes to be delivered. The actual disk space used depends on your PC’s file system. For example, if you are using a machine with FAT 16-type file partitioning, the unzipped files may take up as much as 10 times more disk space than indicated.

If a device family has multiple device sets, common device files (device library files, shared data files, etc.) are installed automatically when any of the sets is selected. For example, if you check only the first device set Virtex (XCV50), the common files (6.4 MB) and the files specific to that selection (8.4 MB) are installed for a total size of 14.8 MB (6.4 + 8.4). The common device files are only added in once. If you check the first Virtex device set (8.4 MB) and the second Virtex device set (20.9 MB), the total becomes 35.7 MB (6.4 + 8.4+ 20.9).

The device selections are listed below.

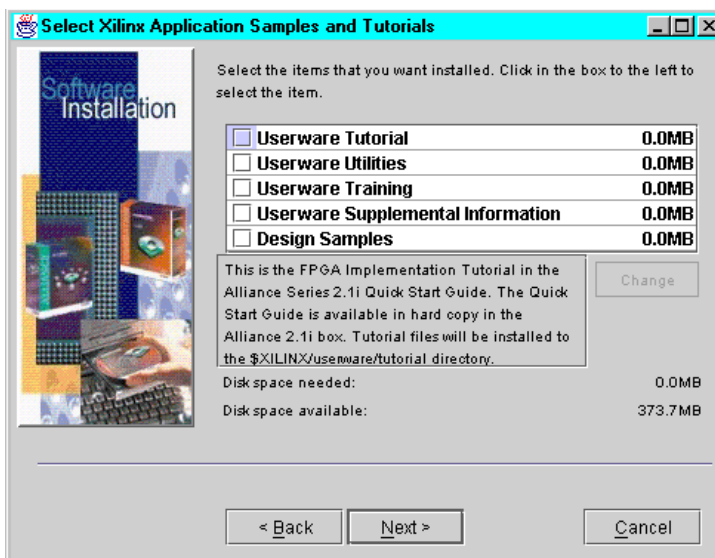
- Spartan (14.4 MB)  
XCS05, XCS10, XCS20, XCS30, XCS40
- SpartanXL (48.6 MB)  
XCS05XL, XCS10XL, XCS20XL, XCS30XL, XCS40XL
- Spartan2  
Please contact your FAE for Spartan2 availability.
- Virtex (total for four device sets: 84.5 MB)
  - XCV50 (6.6 MB)
  - XCV100, XCV150, XCV200, XCV300 (19.2 MB)
  - XCV400, XCV600 (21.1 MB)
  - XCV800, XCV1000 (33.0 MB)
  - common device files installed automatically (4.6 MB)

- VirtexE  
Please contact your FAE for VirtexE availability.
- XC400E (total for 2 device sets: 34.1 MB)
  - XC40003E, XC4005E, XC4006E, XC4008E, XC4010E (12.5 MB)
  - XC4013E, XC4020E, XC4025E (12.3 MB)
  - common device files installed automatically (9.3 MB)
- XC4000L (11.9 MB)  
XC4005L, XC4010L
- XC4000EX (17.8 MB)  
XC4028EX, XC4036EX
- XC4000XL (total for 2 device sets: 100.1 MB)
  - XC4002XL, XC4005XL, XC4010XL, XC4012XL (30.6 MB)
  - XC4020XL, XC4028XL, XC4036XL, XC4044XL, XC4052XL, XC4062XL, XC4085XL (44.5 MB)
  - common device files installed automatically (25.0 MB)
- XC4000XV (total for 2 device sets: 120.4 MB)
  - XC40110XV, XC40150XV (42.0 MB)
  - XC40200XL, XC40250XV (48.5 MB)
  - common device files installed automatically (29.9 MB)
- XC4000XLA (total for 2 device sets: 129.0 MB)
  - XC4013XLA, XC4020XLA, XC4028XLA, XC4036XLA (43.9 MB)
  - XC4044XLA, XC4052XLA, XC4062XLA, XC4085XLA (49.1 MB)
  - common device files installed automatically (36.0 MB)
- XC3000A/L, XC31000A/L (8.8 MB)  
XC3020A, XC3030A, XC3042A, XC3064A, XC3090A,  
XC3020L, XC3030L, XC3042L, XC3064L, XC3090L,  
XC3120A, XC3130A, XC3142A, XC3164A, XC3190A, XC3195A,  
XC3142L, XC3190L

- XC5200 (9.3 MB)  
XC5202, XC5204, XC5206, XC5210, XC5215

## Select Xilinx Application Samples and Tutorials

When the Select Xilinx Application Samples and Tutorials screen appears, you can install the application files to use with the tutorial in the *Foundation Series 2.1i Quick Start Guide* and other application-based documentation, tutorials, and design samples.



You can select to install the following additional components.

- Userware Tutorial

These are the files used with the tutorial in the *Alliance Series 2.1i Quick Start Guide*. The files will be installed in the \$XILINX/userware/tutorial folder.

**Note:** This selection is for the Alliance tutorial files only. Select “Design Samples” to install the files to use with the Foundation tutorials.

- **Userware Utilities**  
 These are Boundary Scan files, IBIS models, and utilities that may be used in conjunction with Foundation Series 2.1i tools. The files will be installed in the \$XILINX/userware/utilities folder.
- **Userware Training**  
 These are presentations and training material for the Xilinx software, HDL constructs, using Design Entry tools and other aspects that may be useful when designing into a Xilinx device. The files will be installed to \$XILINX/userware/training.
- **Userware Supplemental Information**  
 These are PDF and HTML files for any appropriate additional Application Notes, design guides, or user guides for this release. They are installed to \$XILINX/userware/pdf and \$XILINX/userware/directory.
- **Design Samples (and Foundation Tutorial Files)**  
 The design samples listed in the “Design Samples and Foundation Tutorial Files” table are installed in the \$XILINX/active/projects directory. The jct\_XXX designs are used in the basic tutorial described in the *Foundation Series 2.1 Quick Start Guide*. The “watch” and “wtut” files are used in the in-depth tutorial available at <http://support.xilinx.com/support/techsup/tutorials/index.htm>.

**Table 4-1 Design Samples and Foundation Tutorial Files**

<b>Project Name</b>	<b>Description</b>
bcd_acc	Simple Verilog project of 4-digit BCD accumulator
calc3ka	Simple calculator performing basic arithmetic and logic operations on 4-bit numbers
filter	Sample implementation of a digital low pass filter
flash	Simple project of the LogiBLOX and Johnson counters
freqm	Simple implementation of a frequency meter
gate	Simple Verilog project of movement direction detector

**Table 4-1 Design Samples and Foundation Tutorial Files**

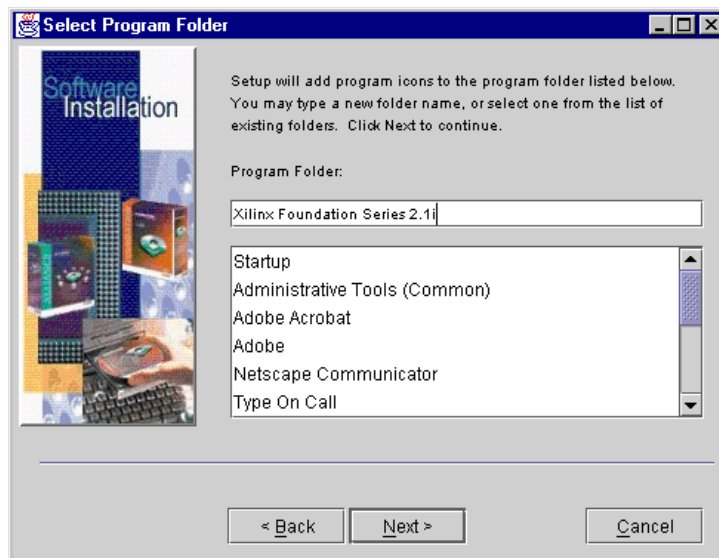
<b>Project Name</b>	<b>Description</b>
hex2bin	Simple project containing HDL code, CoreGEN, LogiBLOX, and schematics
jc2_abl	Simple 4-bit Johnson counter CPLD design (standalone ABEL)
jc2_sabl	Simple 4-bit Johnson counter CPLD design (schematic with ABEL macro)
jc2_sch	Simple 4-bit Johnson counter CPLD design (pure schematic)
jc2_sver	Simple 4-bit Johnson counter CPLD design (schematic with Verilog macro)
jc2_svhd	Simple 4-bit Johnson counter CPLD design (schematic with VHDL macro)
jc2_ver	Simple 4-bit Johnson counter CPLD design (standalone Verilog)
jc2_vhd	Simple 4-bit Johnson counter CPLD design (standalone VHDL)
jct_schf	Simple 4-bit Johnson counter (pure schematic; basic tutorial)
jct_schu	Simple 4-bit Johnson counter (pure schematic; unfinished design for basic tutorial)
jct_verf	Simple 4-bit Johnson counter (standalone Verilog; basic tutorial)
jct_veru	Simple 4-bit Johnson counter (standalone Verilog; unfinished design for basic tutorial)
jct_vhdf	Simple 4-bit Johnson counter (standalone VHDL; basic tutorial)
jct_vhdu	Simple 4-bit Johnson counter (standalone VHDL; unfinished design for basic tutorial)
watch_sc	Stop watch project (schematic; in-depth tutorial)
watchver	Stop watch project (Verilog; in-depth tutorial)
watchvhd	Stop watch project (VHDL; in-depth tutorial)
wtut_sc	Stop watch project (schematic; unfinished design for in-depth tutorial)

**Table 4-1 Design Samples and Foundation Tutorial Files**

Project Name	Description
wtut_ver	Stop watch project (Verilog; unfinished design for in-depth tutorial)
wtut_vhd	Stop watch project (VHDL; unfinished design for in-depth tutorial)

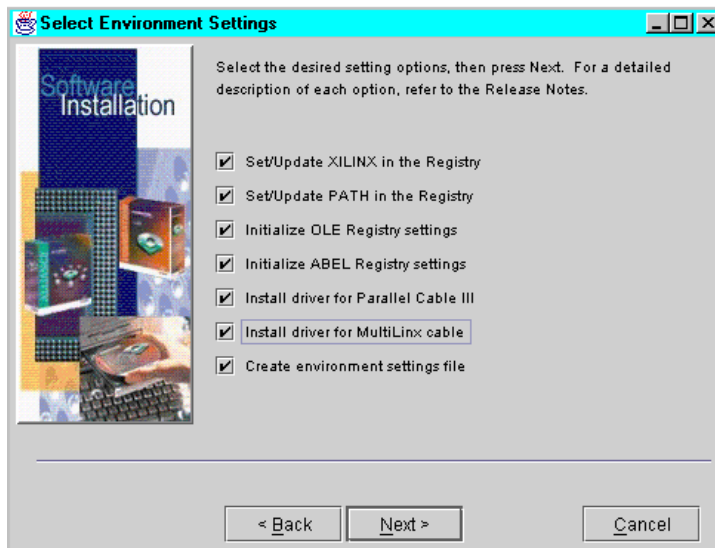
## Select Program Folder

By default, the installation program adds icons to the “Xilinx Foundation Series 2.1i” program folder. You can select to have the Foundation icons added to another existing folder or to change the name of the default program folder. The name entered here appears in the **Start** → **Programs** list on your desktop.



## Select Environment Settings Options

The Environment Settings Options dialog box (Windows 95/98) or Registry Settings Options dialog box (Windows NT) lets you select default option settings for environment variables, your path, and the Registry. By default, all options are selected. Following is a description of each option.



### Set/Update XILINX

If this option is selected, the XILINX variable is set to point to C:\Fndtn as the default or the directory you selected from the Select Foundation Destination Directory screen.

For Windows NT, the XILINX variable is set in the Registry. For Windows 95/98, this variable is set in the autoexec.bat file.

### Set/Update PATH

If this option is selected, the location of the Xilinx software and the DLLs are added to your PATH. This path is the same as the XILINX variable followed by \bin\nt. For Windows NT, the PATH variable is set in the Registry. For Windows 95/98, the PATH is set in the autoexec.bat file. The PATH variable must be set to run the Foundation software.



## Initialize OLE Registry settings

OLE (Object Linking and Embedding) software enhances the transfer of data between programs (for example, between the Project Manager and the FPGA Editor). Xilinx recommends that you select this option. You can also initialize OLE settings by running the command, `revengine /REGISTER`, at a command line prompt from the `%XILINX%\bin\nt` directory.

## Initialize ABEL Registry setting

This option adds registry values that are required to use the ABEL HDL compiler.

## Install driver for Parallel Cable III

Select this option to install the driver for the Parallel Cable III. The parallel cable is required to download bitstreams using the Hardware Debugger (FPGAs) and the JTAG Programmer.

## Install driver for MultiLINX Cable

Select this option to install the driver for the MultiLINX Cable. The MultiLINX cable is the next generation configuration and readback tool for FPGAs and CPLDs.

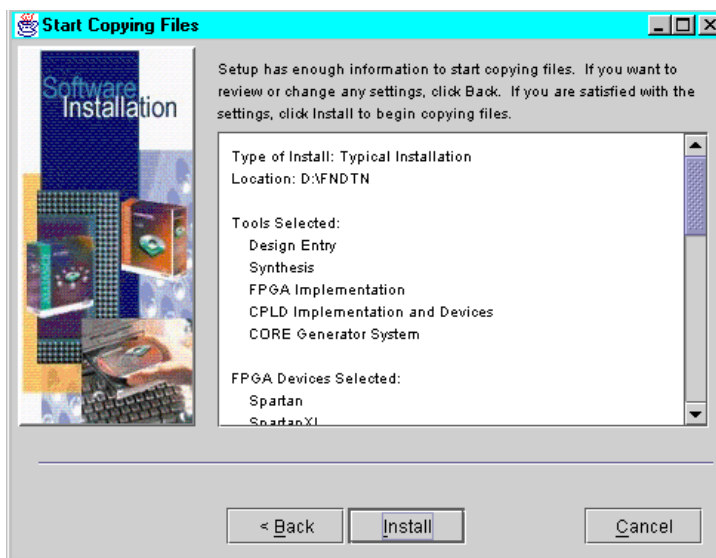
## Create environment settings file

The `xilinx.bat` file, which is created during installation, contains the settings for the `XILINX` and `LM_LICENSE_FILE` variables. The file is located in your installation directory. If necessary, you can run this file to set these variables.

## Check Setup Settings Before Copying Files

Before you instruct the installation program to begin copying files for the installation of your Foundation product, scroll through the Start Copying Files window.

Verify that the items listed are the ones you want set up. To accept the settings, click **Install**. To change any settings, click **Back** to the appropriate screen.



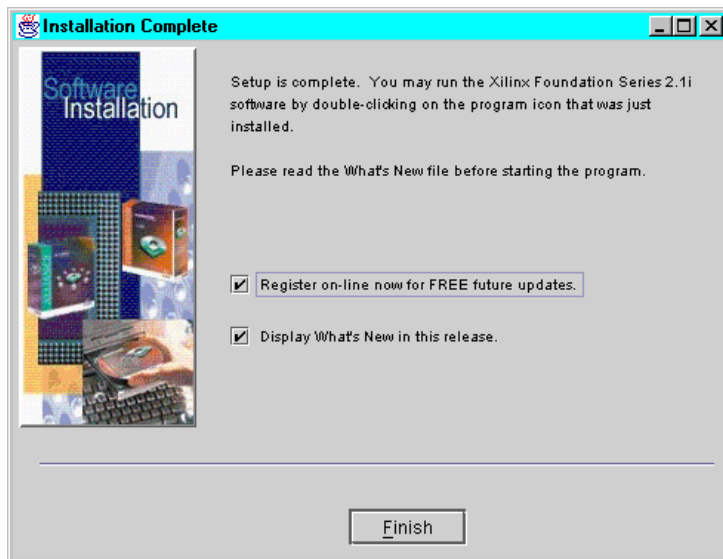
## Copy Files

After you have reviewed the settings, made any necessary changes, and clicked **Install**, at the Start Copying Files window, the install program begins copying files.

## Installation Complete

After all files have been successfully copied, you are presented with a series of screens.

- If you are installing Base Express or Foundation Express, a screen informs you of the status of your license file. New customers have an evaluation license that allows them to begin designing their projects. They need to get the proper authorization to obtain their permanent license. Existing customers need to alter the LM\_LICENSE\_FILE variable to access the 90-day evaluation license just installed on the system. To receive a permanent, full-feature license, both new and existing customers need to follow the instructions in the “Express Software Licensing” chapter. Click **OK** to acknowledge the message.
- When the Installation Complete screen appears, you can choose to view the What’s New file or to register online. Click **Finish** when you have selected the desired options.



- If you installed components that require you to reboot (cable drivers, for example), a screen informs you that a reboot is necessary to activate the changes. Reboot your PC at your convenience.

## Post Installation

### Verify the Xilinx Environment Setup

Verify that the following variables are set in your autoexec.bat file for Windows 95/98 or the Environment tab of System Properties dialog box for Windows NT 4.0. Look under “environment variables” in the Index tab of Windows NT Help to access the System Properties dialog box.

It is assumed that you have loaded the software noted in the previous step to the c:\Fndtn directories on your PC. If the software has been installed in different areas, modify the following statements accordingly.

- The PATH variable sets the overall executable search path. It must include the directories where the Foundation software has been installed. The following command illustrates how to set your path in the autoexec.bat file for Windows 95/98.

```
PATH=C:\FNDTN\BIN\NT;%PATH%
```

For Windows NT 4.0, in the System Properties dialog box, enter the specified text in the Variables and Values fields:

```
Variables: PATH
```

```
Value: C:\FNDTN\BIN\NT
```

```
Variables: XILINX
```

```
Value: C:\FNDTN
```

Click Set in the System Properties dialog box and then click OK.

**Note:** The PATH variable cannot include any previous version of the XACTstep software. Be sure to remove all paths to older software.

- The XILINX variable is used by the Foundation software to locate data files. It must specify the directory where the Foundation software resides. This variable is automatically set up during installation.
- The LM\_LICENSE\_FILE variable directs the design synthesis software to the license files. These files may be placed anywhere as long as this variable points to the license files themselves, not just the directory in which they reside.

For Windows 95/98, enter the following in the autoexec.bat:

For a full-function Express license file:

```
SET LM_LICENSE_FILE=C:\FLEXlm\LICENSE.DAT
```

For a temporary Express license file:

```
SET LM_LICENSE_FILE=%XILINX%\DATA\LICENSE.DAT
```

For Windows NT 4.0, in the System Properties dialog box, enter the specified text in the Variables and Values fields:

For a full-function Express license file:

Variables: LM\_LICENSE\_FILE

Value: C:\FLEXlm\LICENSE.DAT

For a temporary Express license file:

Variables: LM\_LICENSE\_FILE

Value: %XILINX%\DATA\LICENSE.DAT

Click **set** in the System Properties dialog box and then click **OK**.

## Install the Documentation CD (Optional)

The Foundation Series 2.1i Documentation CD contains online books to accompany the tools and devices you just installed with the Foundation Series 2.1i Design Environment CD. Refer to the “Documentation” chapter for complete information on documentation available for Foundation 2.1i and for the Documentation CD installation instructions.

## Begin Designing with Foundation

You are now ready to create and implement Foundation Series designs. Refer to the “Getting Started” chapter for basic Foundation application information.

## **Set Security for Base Express and Foundation Express**

The LM\_LICENSE\_FILE environment variable is used by the FLEXlm software to enable the various components of the Express tools.

If you are not currently running FLEXlm software, the installation program will define the variable. Xilinx recommends you accept the default destination directory in the variable, %XILINX%\data for a temporary Express license file. The recommended location for a full-function Express license file is c:\FLEXlm.

If your PC already has the LM\_LICENSE\_FILE variable defined, the installation program does not modify the variable. After completing a Base Express or Foundation Express installation, read the “Express Software Licensing” chapter.

## PC Lab Installation

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This chapter describes the PC Lab Installation for device download tools only. If you intend to use a second PC (other than the PC you use to design with Foundation) to download completed Foundation designs to a physical device, you need to install only the Foundation device download programs on the second PC. This is known as a “lab” install.

The Xilinx device download tools are the JTAG Programmer, Hardware Debugger, and the PROM File Formatter. All three of these are installed by the PC Lab Installation. In addition, the PC Lab Installation automatically includes the necessary device files for all of the Xilinx devices (both CPLDs and FPGAs) in this release.

**Note:** A CD Key and serial number are *not* required for this type of installation.

### Start the Installation

To start the installation, insert the Design Environment CD into the CD-ROM drive.

If your system has the Auto Run feature enabled, the Foundation installer starts automatically.

If you do not have the Auto Run enabled on your system, select **Start** → **Run**. Type **d:setup.exe** in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)

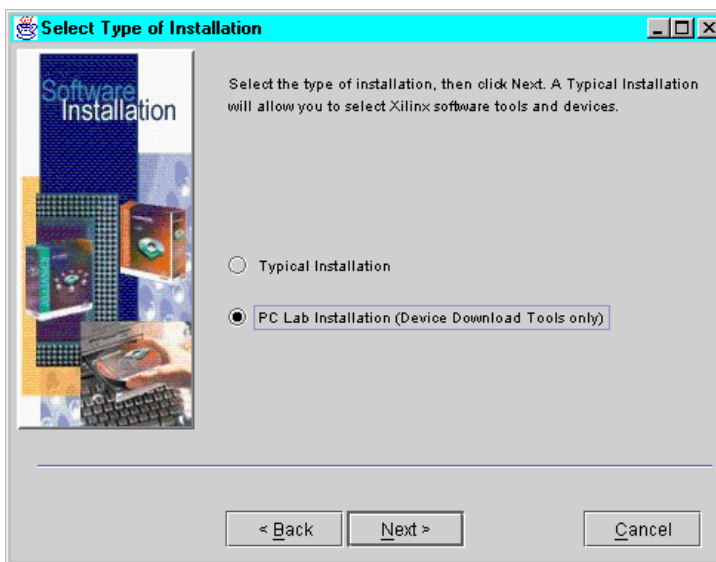
The first screen is the Welcome Screen. Click **Next** when you are ready to proceed with the installation.

The installation screens at the beginning of the update process are the same screens described in the Typical Installation chapter. Refer to that chapter for details on the following screens:

- **Welcome**  
Click **Next** when you are ready to proceed with the installation.
- **Identify Browser Location**  
Select one of the displayed options and then click **Next** to continue.
- **Software License Agreement**  
You must indicate your acceptance of the license agreement by clicking the license agreement box at the bottom of the screen. The box must be checked before you can click **Next** to continue with the installation.

## Select Type of Installation

When the Type of Install screen appears, select the **PC Lab Installation (Device Download Tools Only)**. (Refer to the “Typical Installation” chapter for information on that option.)





The PC Lab Installation option installs three tools: the Hardware Debugger, PROM File Formatter, and JTAG Programmer components. A description of each of these tools follows.

### **Hardware Debugger**

The Hardware Debugger is a graphical interface that allows you to download an FPGA design to a device, verify the downloaded configuration, and display the internal states of the programmed device.

### **PROM File Formatter**

The PROM File Formatter is available for FPGA designs only. The PROM File Formatter provides a graphical user interface that allows you to do the following.

- Format BIT files into a PROM file compatible with Xilinx and third-party PROM programmers
- Concatenate multiple bitstreams into a single PROM file for daisy chain applications
- Store several applications in the same PROM file

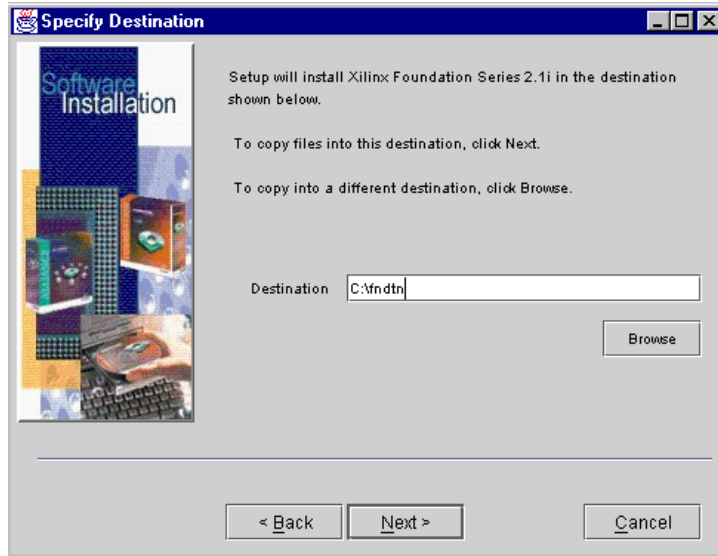
### **JTAG Programmer**

The JTAG Programmer downloads, reads back, and verifies FPGA (except for XC3000A/L and XC31000A/L families) and CPLD design configuration data through the JTAG port. It can also perform functional tests on any device and probe the internal logic states of your design.

## Specify Destination

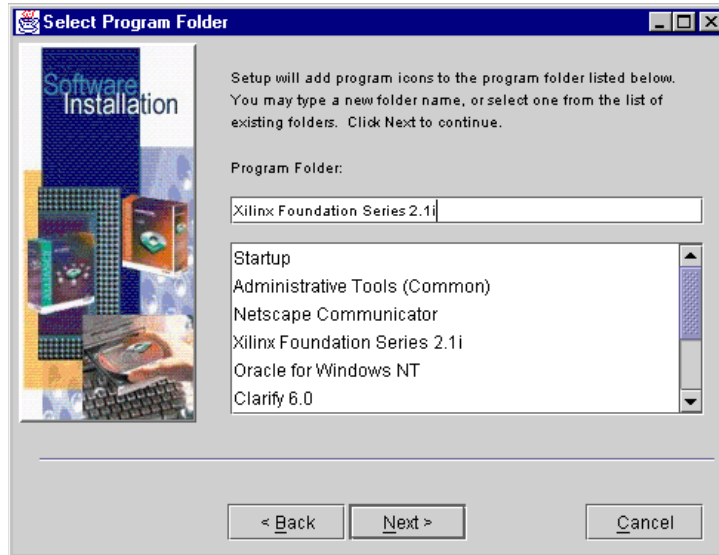
After you click **Next** at the Select Type of Installation screen for a PC Lab Installation, you are given the option of installing the product in the default folder `c:\fndtn` or choosing another folder. Click **Browse** to choose another folder, if desired.

Click **Next** when the desired Destination Folder is selected.



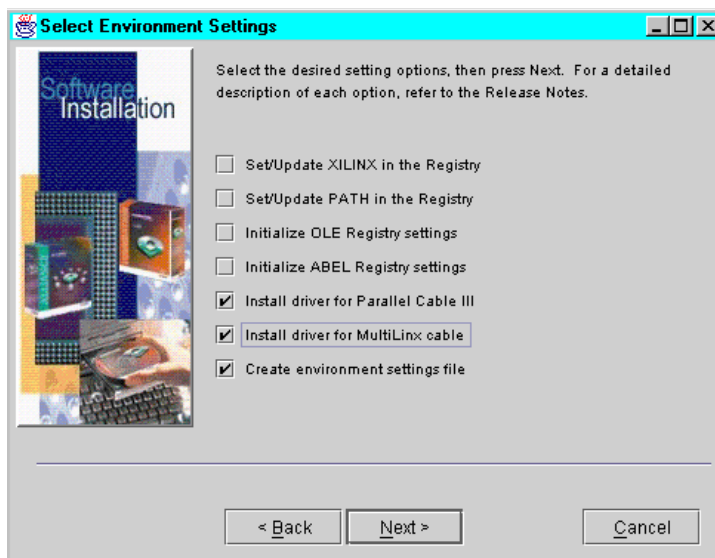
## Select Program Folder

By default, the installation program adds icons to the “Xilinx Foundation Series 2.1i” program folder. You can select to have the Foundation icons added to another existing folder or to change the name of the default program folder. The name entered here appears in the **Start** → **Programs** list on your desktop.



## Select Environment Settings

The Select Environment Settings screen allows you to select default option settings for environment variables, your path, and the Registry. For a Device Download Tools Only installation, three options apply: Install driver for Parallel Cable III, Install driver for MultiLINX cable, and Create environment settings file. These options are selected by default.



### Install Driver for Parallel Cable III

Select this option to install the driver for the Parallel Cable III. The parallel cable is required to download bitstreams using the Hardware Debugger (FPGAs) and the JTAG Programmer.

### Install Driver for MultiLINX Cable

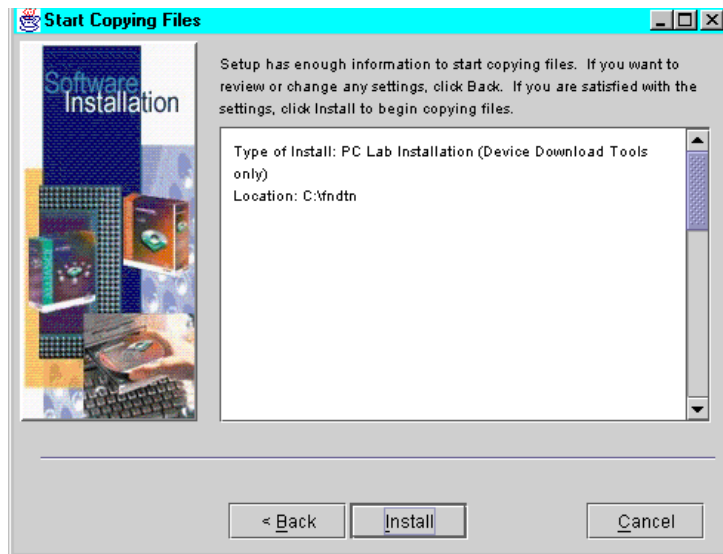
Select this option to install the driver for the MultiLINX cable. The MultiLINX cable is a device for configuring and verifying Xilinx FPGAs and CPLDs. The MultiLINX cable hardware communicates with the host through the Universal Serial Bus (USB) port or an RS-232 interface. Additional flying wires support the various configuration modes available on Xilinx configuration cables.

## Create Environment Settings File

The `xilinx.bat` file, which is created during installation, contains the settings for the `XILINX`, `XILINX_CD`, `PATH`, and `LM_LICENSE_FILE` variables. The file is located in `%XILINX%`. If necessary, you can double click on this file to set these variables.

## Start Copying Files

After you have reviewed the settings, made any necessary changes, and clicked **Install**, at the Start Copying Files window, the install program begins copying files.



## Complete the Setup

When the Setup Complete screen appears, you can choose to view the What's New file and/or to register online. Click the appropriate selection buttons and then click **Finish** to proceed.

A message informs you whether a reboot is needed. Reboot your PC at your convenience if a reboot is necessary.



## Upgrading to Foundation 2.1i

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If you currently have version 1.5i or earlier of the Foundation Series software, you can upgrade to version 2.1i and have your 1.5i projects converted to 2.1i projects when they are opened in 2.1i. A 1.5i project can also be archived in 1.5i format before it is converted.

Foundation Series 1.4 and earlier (XACTStep M1 or XACTStep6) projects are *not* supported in the Foundation Series 2.1i project manager. They must be migrated into F1.5i if they are to be brought into 2.1i.

### Beginning the Update

To upgrade a Typical Installation of your current Foundation Series software, insert the Foundation Series 2.1i Design Environment CD into the CD-ROM drive on your PC.

If your system has the Auto Run feature enabled, the Foundation installer starts automatically.

If you do not have the Auto Run enabled on your system, select **Start** → **Run**. Type **d:\setup.exe** in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)

The first screen is the Welcome Screen. Click **Next** when you are ready to proceed with the installation.

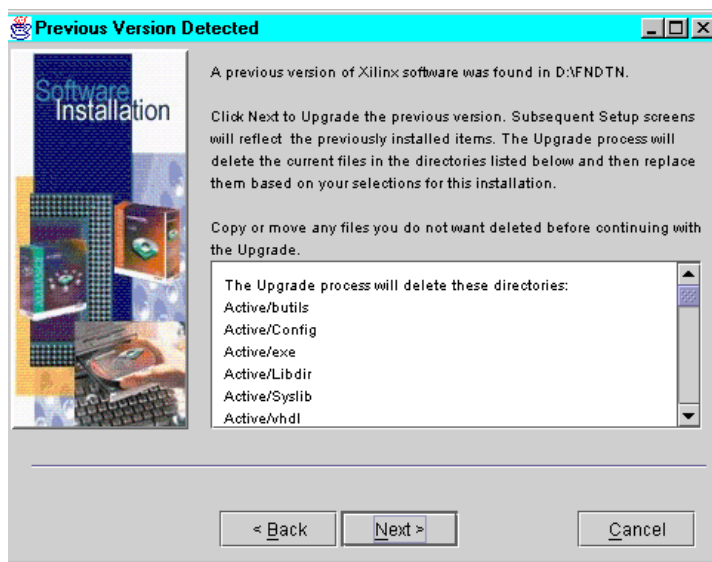
The installation screens at the beginning of the update process are the same screens described in the Typical Installation chapter. Refer to that chapter for details on the following screens:

- Welcome
- Identify Browser Location

- Software License Agreement
- Select Type of Installation
- User Information
- Specify Destination

## Previous Version Detected

After you specify the destination for the Foundation Series 2.1i installation, the Previous Version Detected screen appears.



**Warning:** All files in the directories listed in the white box at the bottom of the screen *will be deleted* when you click **Install** at the Start Copying Files screen. They will then be replaced with the 2.1i version of the files.

Scroll through the directories listed in the box at the bottom of the screen. If there are any directories listed there that you do not want deleted, you must rename the directory or copy the files you want to save to a new directory *before* continuing.



## Completing the Update

The installation screens that appear after you click **Next** at the Previous Version Detected screen are the same screens as described in the Typical Installation chapter. The items selected by default on the following screens, however, will reflect what you had installed before you began the update to Foundation Series 2.1i. You can modify the default selections by selecting or de-selecting the boxes to the left of an item.

- Select Tools to Install
- Select FPGA Devices to Install
- Select Xilinx Application Samples and Tutorials
- Select Program Folder
- Select Environment Settings Options

**Warning:** If you did not review the list of directories to be deleted shown on the Previous Version Detected screen, click the **Back** and review that list *before* continuing.

Click **Install** at the Start Copying Files screen to replace your previously installed version of Foundation with the Foundation Series 2.1i files.



## Documentation

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Foundation Series 2.1i documentation is available from multiple sources and in multiple formats.

The 2.1i software manuals are available in both HTML and Adobe Acrobat PDF formats on the Xilinx web site at <http://support.xilinx.com> and on the provided Documentation CD. The Docsan documentation index adds enhanced searching and indexing capabilities to your HTML browser. You can view the books and use the documentation index directly from the web site or the Documentation CD. Or, you can install them on your PC.

Hard copy books, online help, tutorials, and a multimedia quick start demo are also provided.

## Prerequisites

You need a Java-enabled HTML browser such as Netscape Navigator 4.5 or Internet Explorer 4.0 to view the online books and use the Docsan documentation index. You need the Adobe Acrobat Reader 3.0 to view and/or print the PDF files. You can install these programs from either the Foundation Series 2.1i Design Environment CD or the Foundation Series 2.1i Documentation CD.

## Installing Netscape Navigator 4.5

If your PC does not currently have an HTML browser or if you want to upgrade your browser, you can install Netscape Navigator 4.5 as follows.

1. Insert the Foundation Series 2.1i Documentation CD or Design Environment CD into your PC's CD-ROM drive.
2. Select **Start** → **Run**.

3. Type `d:\DocTools\Netscape\english\cc32e451.exe` in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)
4. Follow the instructions in the Netscape Navigator installation program.

## Installing Adobe Acrobat Reader 3.01

If your PC does not currently have Adobe Acrobat Reader 3.0 or if you want to upgrade your installation, you can install Adobe Acrobat Reader 3.01 as follows.

1. Insert the Foundation Series 2.1i Documentation CD or Design Environment CD into your PC's CD-ROM drive.
2. Select **Start** → **Run**.
3. Type `d:\DocTools\Acrobat\english\ar32e301.exe` in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)
4. Follow the instructions in the Adobe Acrobat Reader installation program.

## Hard Copy Documentation

The *Foundation Series 2.1i Installation Guide and Release Notes* (this document) describes new features, supported devices, installation and security procedures, and the most critical known issues.

The *Foundation Series 2.1i Quick Start Guide* provides an overview of the features and additions to Xilinx's 2.1i software. This document describes new features for Foundation 2.1i, design entry tools, and design implementation tools. It includes a basic tutorial that provides an overview of the phases in the Foundation design development process. This book is also available in the online book collection.

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## Online Help System

Online help is automatically installed along with the tools you install from the Foundation Series 2.1i Design Environment CD. Context-sensitive help is available from the Help menu of each program.

### Direct Link to Xilinx Support Web Site

Project Manager online help in the Foundation Series 2.1i software includes direct links to the Xilinx customer service and support web site at <http://support.xilinx.com>. To access the web site from the Project Manager, select **Help** → **Xilinx on the Web**. This site contains links to the Answers Search, Software Updates, Expert Journals, Application Notes and the online manuals.

### Direct Link to Online Documentation

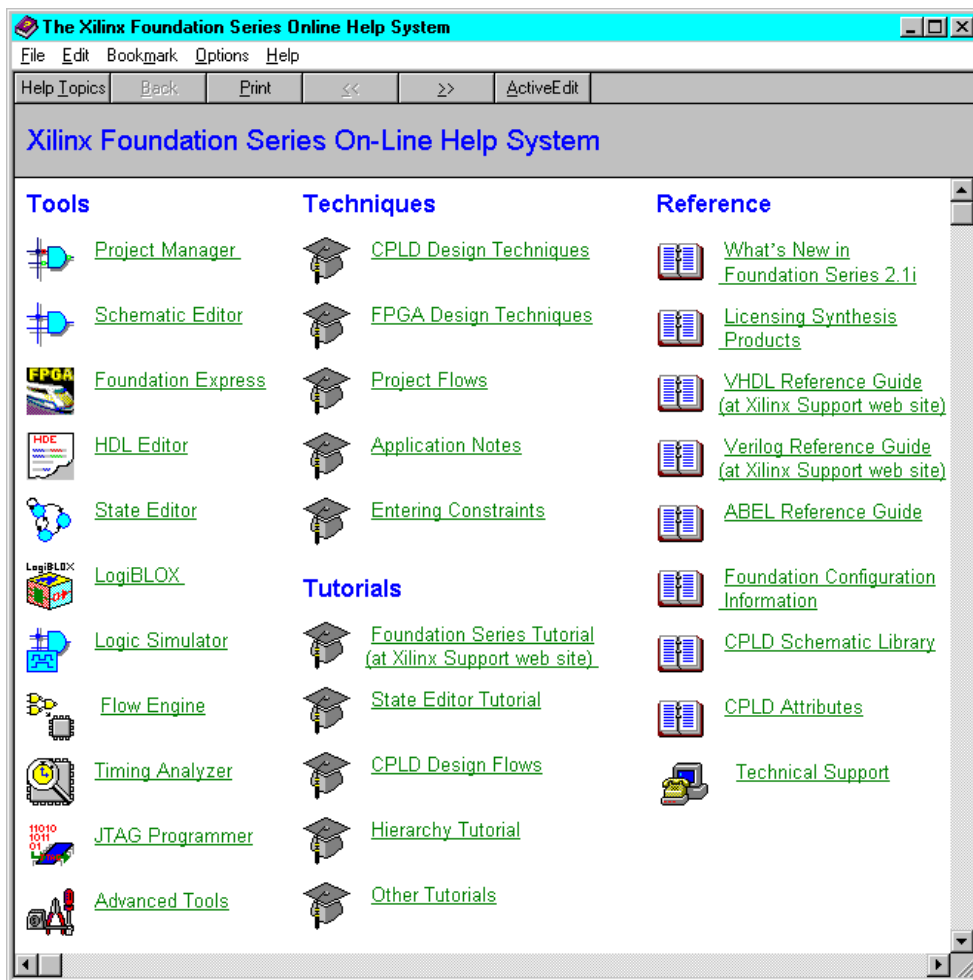
Project Manager online help includes a direct link to the software manuals for this release. To access the Docsan index and manuals from the Project Manager, select **Help** → **Online Documentation**. If the manuals are not installed on your PC, you can access them on the Xilinx Support web site or the Documentation CD via the Online Documentation option.

### Umbrella Help

Foundation includes an “umbrella” help system called the Xilinx Foundation Series On-Line Help System. It contains help topics covering all of the design entry and implementation tools provided in the product plus additional information. This “umbrella” help system contains in-depth information essential for designing with FPGAs and CPLDs, including the following topics:

- CPLD design techniques
- FPGA design techniques
- Application notes
- Several tutorials
- Reference information on the HDL languages, CPLD schematic library and attributes, and Foundation configurations

You can invoke the “umbrella” help system (shown in the following figure) by selecting **Help** → **Foundation Help Contents** from the Project Manager menu bar or from the Xilinx Foundation Series program group.



## Tutorials

In addition to the basic tutorial (jcount) in the *Foundation Series 2.1i Quick Start Guide*, an in-depth tutorial (the WATCH tutorial) and the necessary files to use with it are available at <http://support.xilinx.com/support/techsup/tutorials/index.htm>.

## Multimedia Quick Start Demo

A multimedia demo of the Foundation product features is included on the Foundation Series 2.1i Documentation CD. You can only run the demo from the CD. You cannot install it to your PC's hard drive.

To run the demo from the CD, do the following.

1. Insert the Foundation Series 2.1i Documentation CD into your PC's CD-ROM drive.
2. Select **Start** → **Run**.
3. Type **d:fndtn\_mmd.exe** in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the "d" drive, substitute the appropriate drive designation.)

The demo is also accessible from the Xilinx program folder after you install the Foundation Series 2.1i Design Environment software as follows.

1. Insert the Foundation Series 2.1i Documentation CD into your PC's CD-ROM drive.
2. Select **Start** → **Programs** → **Xilinx Foundation Series 2.1i** → **Multimedia Foundation Demo**.

## Additional Resources

For additional information and documentation, go to <http://support.xilinx.com>. The following table lists some of the resources you can access from this page. You can also directly access some of these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging <a href="http://support.xilinx.com/support/techsup/tutorials/index.htm">http://support.xilinx.com/support/techsup/tutorials/index.htm</a>
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at <a href="http://support.xilinx.com/support/searchtd.htm">http://support.xilinx.com/support/searchtd.htm</a>
Application Notes	Descriptions of device-specific design techniques and approaches <a href="http://support.xilinx.com/apps/appsweb.htm">http://support.xilinx.com/apps/appsweb.htm</a>
Data Book	Pages from <i>The Programmable Logic Data Book</i> , which describe device-specific information on Xilinx device characteristics, including read-back, boundary scan, configuration, length count, and debugging <a href="http://support.xilinx.com/partinfo/databook.htm">http://support.xilinx.com/partinfo/databook.htm</a>
XCell Journal	Quarterly journal for Xilinx programmable logic users <a href="http://support.xilinx.com/xcell/xcell.htm">http://support.xilinx.com/xcell/xcell.htm</a>
Tech Tips	Latest news, design tips, and patch information on the Xilinx design environment <a href="http://support.xilinx.com/support/techsup/journals/index.htm">http://support.xilinx.com/support/techsup/journals/index.htm</a>

The *XACT Conversion Guide* is available on the Xilinx web site ([http://www.xilinx.com/techdocs/htm\\_index/docs\\_M1.htm](http://www.xilinx.com/techdocs/htm_index/docs_M1.htm)). This guide explains how to migrate existing design files created by XACT-Step V6.x software for use with Xilinx M1 software.

## Foundation Series 2.1i Online Books

This section describes the books included in the Foundation Series 2.1i online book set and how to access them. Please review the list to become familiar with the available Xilinx documentation.

You only need to run the installation program on the Documentation CD if you want to install the Docsan documentation viewer and books on your PC. Refer to the “installing Docsan” section for more information. If you do not want to use the Docsan documentation index, the HTML and PDF files can be copied from the Documentation CD to your PC, if desired.



## Online Book Access

Some of the ways you can access the Foundation 2.1i online books are described below. All methods require that an appropriate HTML browser or Adobe Acrobat Reader is already installed on your PC. Refer to the “Prerequisites” section in this chapter for information on installing these tools if necessary.

### From the Start Menu

If you installed the Docsan index and book collection from the Documentation CD, you can open the Docsan index by selecting **Start** → **Programs** → **Xilinx Foundation Series 2.1i** → **Online Documentation**. The Docsan tool’s Help feature includes links to the PDF files if you want to print the files.

### From the Foundation Project Manager

You can access the HTML books directly from Foundation’s Project Manager as described below.

- Select **Help** → **Online Documentation** from the Project Manager window.
- If the manuals are installed on your PC, the Docsan index/search tool opens immediately for you to search/read the collection.
- If the manuals are not installed on your PC, a window appears that includes the following.
  - A link to the Docsan manuals on the Xilinx support web site
  - A link to the PDF files on the Xilinx support web site (for downloading the files)
  - Instructions on installing the manuals onto your PC
  - Instructions on reading or printing the manuals from the Documentation CD

### From the Documentation CD with Docsan Indexing

To view the HTML books directly from the Documentation CD using the Docsan enhanced documentation indexing and searching, do the following.

1. Insert the Documentation CD into your PC’s CD-ROM drive.

2. Select **Start** → **Run**.
3. Type **d:\index.htm**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)
4. Refer to the “Using the Docsan Documentation Index” section of the “Getting Started” chapter for information on using the Docsan documentation index. The documentation index includes links to the PDF versions of the books.

### **From the Xilinx Web Site with Docsan Indexing**

To view the HTML books on the Xilinx support web site using the Docsan enhanced documentation indexing and searching, do the following.

1. Open your internet access program in the usual manner.
2. Type **http://support.xilinx.com** in the Netsite locator box.
3. When the SUPPORT.XILINX.COM home page appears, click on the **Library** tab and then click on **SW Manuals** to open the Docsan documentation index.
4. Refer to the “Using the Docsan Documentation Index” section of the “Getting Started” chapter for information on using the documentation index. The documentation index includes links to the PDF versions of the books.

### **From the Documentation CD without Docsan Indexing**

To view the HTML books directly from the Documentation CD using just your HTML browser, do the following

1. Insert the Documentation CD into your PC’s CD-ROM drive.
2. Select **Start** → **Programs** → **Windows Explorer** (or **Windows NT Explorer**).
3. When the Explorer window appears, go to **d:**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.) Then refer to “Foundation Online Books” table for the location of the top file for each HTML book and double click on that file.

For example, to open the Libraries Guide, go to d:/data/foundation/lib and double click lib.htm. The first page of the Libraries Guide appears in your browser window.

## PDF Files on the Documentation CD

To view or print PDF files from the Documentation CD, do the following.

1. Start the Acrobat Reader by selecting **Start** → **Adobe Acrobat** → **Acrobat Reader**.
2. In the Acrobat Reader window, select **File** → **Open**.
3. Insert the Documentation CD into your PC's CD-ROM drive.
4. In the Acrobat Reader's Open dialog box, click the arrow on the right side of the "Look in" box and select your PC's CD-ROM drive from the pulldown menu that appears.
5. Double click the **Print** folder on the Documentation CD's directory list.
6. Refer to "Foundation Online Books" table" for the PDF filename of the desired book and double click on that filename to open the file in the Acrobat Reader.

For example, to open the Libraries Guide, go to d:/print and double click libguide.pdf. The first page of the Libraries Guide appears in your browser window.

## Online Book Descriptions

The table in this section categorizes and describes each of the Foundation Series 2.1i online books. It includes where each book is located on the Documentation CD. If you are using the Docsan documentation index, the HTML location information is not needed.

**Note:** The *CORE Generator User Guide* is not currently part of the online book collection. It is an Adobe Acrobat file (.pdf) that can be accessed from the CORE Generator Help menu (**Help** → **Online Documentation**.)

**Table 7-1 Foundation Online Books**

Title	Description/Location on Documentation CD <sup>a</sup>
<b>Foundation-Specific Online Books:</b>	
<i>Foundation Series 2.1i Quick Start Guide</i>	<p>This book gives an overview of the features and additions to Xilinx's Foundation 2.1i product.</p> <p>HTML: <a href="data/fndtn/fqs/fqs.htm">data/fndtn/fqs/fqs.htm</a>            PDF: <a href="print/qsprint.pdf">print/qsprint.pdf</a></p>
<i>Foundation Series 2.1i User Guide</i>	<p>This book describes the Foundation design methodologies, design entry tools, plus functional and timing simulation. It briefly describes the Xilinx design implementation strategy and theory.</p> <p>HTML: <a href="data/fndtn/fsu/fsu.htm">data/fndtn/fsu/fsu.htm</a>            PDF: <a href="print/fsuguide.pdf">print/fsuguide.pdf</a></p>
<i>Verilog Reference Guide</i>	<p>This manual describes how to use Xilinx Foundation Express to translate and optimize a Verilog HDL description into an internal gate-level equivalent.</p> <p>HTML: <a href="data/fndtn/ver/ver.htm">data/fndtn/ver/ver.htm</a>            PDF: <a href="print/ver.pdf">print/ver.pdf</a></p>
<i>VHDL Reference Guide</i>	<p>This manual describes how to use Xilinx Foundation Express to compile VHDL designs.</p> <p>HTML: <a href="data/fndtn/vhd/vhd.htm">data/fndtn/vhd/vhd.htm</a>            PDF: <a href="print/vhdl.pdf">print/vhdl.pdf</a></p>
<b>Design Entry Online Reference Books:</b>	
<i>Libraries Guide</i>	<p>The Libraries Guide describes the Xilinx Unified Library components and the attributes and constraints that can be applied to designs.</p> <p>HTML: <a href="data/common/lib/lib.htm">data/common/lib/lib.htm</a>            PDF: <a href="print/libguide.pdf">print/libguide.pdf</a></p>
<i>LogiBLOX Guide</i>	<p>This manual describes Xilinx's LogiBLOX program, a tool used to create high-level modules for insertion into a schematic or HDL-based design, primarily for FPGA architectures.</p> <p>HTML: <a href="data/common/lbk/lbk.htm">data/common/lbk/lbk.htm</a>            PDF: <a href="print/lblox.pdf">print/lblox.pdf</a></p>

Table 7-1 Foundation Online Books

Title	Description/Location on Documentation CD <sup>a</sup>
<b>Synthesis-Related Online Books:</b>	
<i>Synthesis and Simulation Design Guide</i>	<p>This manual provides a general overview of designing FPGAs with Hardware Description Languages (HDLs). It includes design hints for the novice HDL user, as well as for the experienced user who is designing FPGAs for the first time.</p> <p>HTML: <a href="#">data/common/sim/sim.htm</a>  PDF: <a href="#">print/gensim.pdf</a></p>
<b>Implementation-Related Online Books:</b>	
<i>Constraints Editor Guide</i>	<p>This book explains how to use the Xilinx Constraints Editor GUI to create implementation constraints.</p> <p>HTML: <a href="#">data/common/cst/cst.htm</a>  PDF: <a href="#">print/cst_edit.pdf</a></p>
<i>Design Manager/Flow Engine Guide</i>	<p>This book describes using the Xilinx Design Manager and Flow Engine GUIs and shows the implementation options for all Xilinx devices. It also describes the interaction with other Xilinx design implementation GUIs.</p> <p>HTML: <a href="#">data/common/dmf/dmf.htm</a>  PDF: <a href="#">print/dmfe.pdf</a></p>
<i>Development System Reference Guide</i>	<p>This book describes the implementation programs in the Xilinx Development System. It covers all program functions, command line options, and files that are generated by these programs. It also contains an in-depth explanation of timing constraints.</p> <p>HTML: <a href="#">data/common/dev/dev.htm</a>  PDF: <a href="#">print/dev_ref.pdf</a></p>
<i>FPGA Editor Guide</i>	<p>This book explains how to use the FPGA Editor GUI, to modify placement and routing, to use constraints, and to verify timing.</p> <p>HTML: <a href="#">data/common/fpg/fpg.htm</a>  PDF: <a href="#">print/fpedit.pdf</a></p>
<i>Floorplanner Guide</i>	<p>This book explains how to use the Floorplanner GUI to place logical design symbols into target FPGAs.</p> <p>HTML: <a href="#">data/common/flr/flr.htm</a>  PDF: <a href="#">print/fplan.pdf</a></p>

**Table 7-1 Foundation Online Books**

Title	Description/Location on Documentation CD <sup>a</sup>
<i>Hardware User Guide</i>	<p>This manual explains how to connect and use the MultiLINX Cable, Parallel Cable II, and XChecker Cable for downloading designs. It also describes FPGA and CPLD demonstration boards.</p> <p>HTML: data/common/hug/hug.htm  PDF: print/huguide.pdf</p>
<i>Timing Analyzer Guide</i>	<p>This guide describes Xilinx's Timing Analyzer program, a GUI that performs static timing analysis of a mapped FPGA or CPLD design.</p> <p>HTML: data/common/tme/tme.htm  PDF: print/timing.pdf</p>
<b>Device Programming Online Books:</b>	
<i>Hardware Debugger Guide</i>	<p>This manual describes Xilinx's Hardware Debugger GUI tool used for configuring and debugging FPGA devices. It explains how to download, readback, and verify FPGA devices using Xilinx cables.</p> <p>HTML: data/common/hdb/hdb.htm  PDF: print/hdebug.pdf</p>
<i>JTAG Programmer Guide</i>	<p>This manual explains Xilinx's JTAG program, which is used to download, read back, and verify design configuration data for FPGAs and CPLDs.</p> <p>HTML: data/common/jtg/jtg.htm  PDF: print/jtag.pdf</p>
<i>PROM File Formatter Guide</i>	<p>This manual explains how to use the PROM File Formatter GUI, how to format bitstream files into HEX, and how to program a PROM device.</p> <p>HTML: data/common/pff/pff.htm  PDF: print/prom_fmt.pdf</p>

a.If you use the Docsan documentation index, it will lead you to the book and format you need. The HTML and PDF locations are only provided here if, for some reason, you chose not to use the Docsan documentation index.

## Installing the Docsan Documentation Index and Books

If internet response time or availability of the Documentation CD in your CD-ROM drive is an issue, you can install the Docsan documentation index and the Foundation 2.1i online books to your PC's hard drive.

### Prerequisites

Before starting the installation, ensure that your PC meets the requirements described in the “System Requirements” chapter.

You *must* install the Foundation Series 2.1i software using the Design Environment CD *before* you install the online book collection.

The Docsan index and the books are automatically installed to the same destination location identified during the Design Environment installation. The Documentation CD setup program does *not* include an option to install the books elsewhere.

### Starting the Documentation Installation

To start the installation, do the following.

1. Insert the Foundation Series 2.1i Documentation Series CD into the CD-ROM drive.
2. Select **Start** → **Run**. Type **d:\setup.exe** in the Open field of the Run window and click **OK**. (If your CD-ROM drive is not the “d” drive, substitute the appropriate drive designation.)

**Note:** The Documentation CD does not have an auto run installation. Even if you have Auto Run enabled on your PC, you must manually start the installation.

### Welcome Screen

When the Welcome screen appears, click **Next** to proceed with the installation.



Click **Next** when you are ready to proceed with the installation.

The installation screens at the beginning of the update process are the same screens described in the Typical Installation chapter. Refer to that chapter for details on the following screens:

## Identify Browser Location

Identify the browser you want to use with Foundation Series 2.1i. If you do not have a Java-enabled HTML browser installed, you can initiate the Netscape Navigator installation program from this screen.

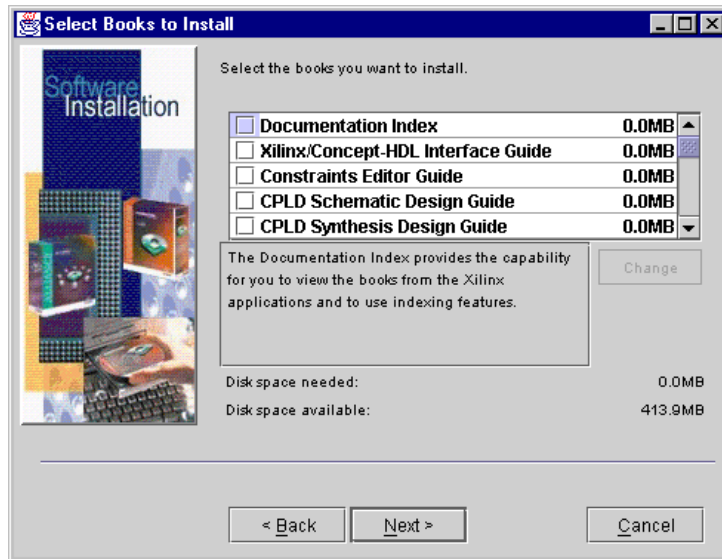
Refer to the “Identify Browser Location” section of the “Typical Installation” chapter for details and example of this screen.

## Select Books to Install

At the Select Books to Install screen, you can select the documentation features you want installed on your PC. By default, the documentation index and all books are installed.

**Note:** If you choose not to install all of the books, the Docsan search function will return “not found” warnings.





## Completing the Installation

The installation screens to complete the Documentation CD installation are the same screens described in the Typical Installation chapter. Refer to that chapter for details on the following screens:

- Select Program Folder

By default, the installation program adds icons to the “Xilinx Foundation Series 2.1i” program folder. You can select to have the Foundation icons added to another existing folder or to change the name of the default program folder. The name entered here appears in the **Start**→**Programs** list on your desktop. Click **Next** when you are ready to continue.

- Start Copying Files

Before the installation program begins copying files for the installation, scroll through the Start Copying Files window. After you have reviewed the settings, made any necessary changes, and clicked **Install**, at the Start Copying Files window, the install program begins copying files.

## **Begin Using the Documentation Index**

Refer to the “Getting Started” chapter for information on using the online documentation enhanced search and index.

## Getting Started

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This chapter gives an overview of the Foundation Project Manager and explains how to start the Foundation software. It also gives an overview on how to open and use the Docsan search index with your HTML browser.

### Foundation 2.1i Projects

To organize your work, Foundation groups all related files into separate logical units called projects. Schematic, HDL, and Finite State Machine (FSM) designs must be defined as elements in a project. The associated libraries as well as netlists, bitstream files, reports, and configuration files are all part of the project.

Each project is stored in a separate directory called the project working directory. The location of the project working directory is specified when the project is created. The name of the project working directory is the same as the name of the project.

A Foundation Series 2.1i project can be either a Schematic Flow project or an HDL Flow project. If you are using the Base or Standard products, only the Schematic Flow is available to you. Both flows are available to Base Express and Foundation Express users.

### Schematic Flow vs HDL Flow

Schematic Flow projects consist of top-level schematic, ABEL, or State Machine designs. The top-level design can have any number of underlying schematic, HDL, LogiBLOX, ABEL, or Finite State Machine (FSM) macros. Although individual modules may require some form of synthesis, the entire project is not synthesized and the netlist that is exported for implementation is not optimized before implementation as in an HDL Flow project.

HDL Flow projects consist of VHDL, Verilog, schematic, or state machine source files. These projects include a synthesis phase. All HDL designs and modules below the top-level file designated during the synthesis phase are elaborated and optimized. The main difference between the Schematic Flow and the HDL Flow is that the HDL Flow synthesizes the complete design optimizing across module boundaries. The Schematic Flow uses a bottom up methodology where each HDL module is synthesized individually.

**Note:** The HDL Flow is available only in Base Express and Foundation Express.

## Project Manager

The Project Manager, the overall project management tool, contains the Foundation Series tools used in the design process. It is through the Project Manager that you access the tools for the design process from design entry tools to device programming.

The Project Manager performs the following functions:

- Automatically loads all design resources when opening a project
- Checks that all project resources are available and up-to-date
- Illustrates the design process flow
- Initiates applications used in the design process
- Displays error and status messages in the message window
- Provides automated data transfer between various Foundation design tools
- Displays design status information

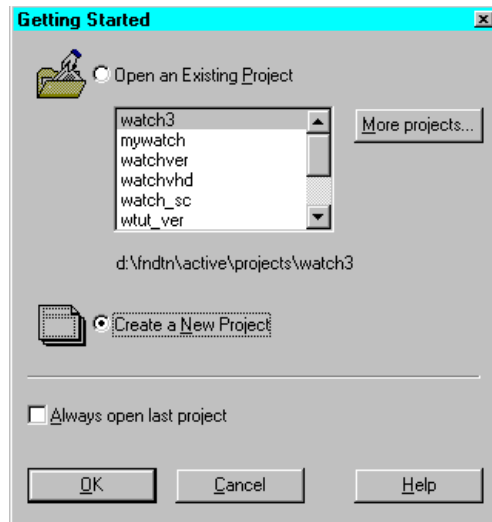
## Starting the Software

As soon as the installation has completed, you are ready to use the Foundation software. To access the Project Manager, double click the Xilinx Foundation Series Project Manager icon.



If you do not have an icon on your desktop, select **Start** → **Programs** → **Xilinx Foundation Series 2.1i** → **Project Manager**.

The Getting Started dialog box appears.



Select **Create a New Project**. The New Project dialog box displays. (If you are upgrading from a previous version of Foundation, please review the information on “Existing F1.5 (or Earlier) Projects” in the “Upgrading to Foundation 2.1i” chapter.)



**Note:** If you select HDL for the Flow, you will not need to specify the device information at this time. It will be removed from the bottom of the screen when HDL is selected. You will specify the target device when the design is synthesized.

After the project is created, the Project Manager window appears. The Flow Chart and tabs that appear on the Project Manager depend on the type of project you created. The Project Manager for Schematic Flow projects is shown at the bottom of this page and the Project Manager for HDL Flow projects is shown on the following page.

The basic design entry tools consist of the Schematic Editor, HDL Editor, and State Editor. These are represented by the three icons on the Design Entry button on the project flow chart. Click on the desired button to open one of the design entry tools.

After design entry, use the buttons on the project flowchart to proceed with your design. A button is grayed out until the project is at a point where that function is appropriate. The Project Manager will prompt for any needed input or processing and keep track of what needs to be done to process your design.

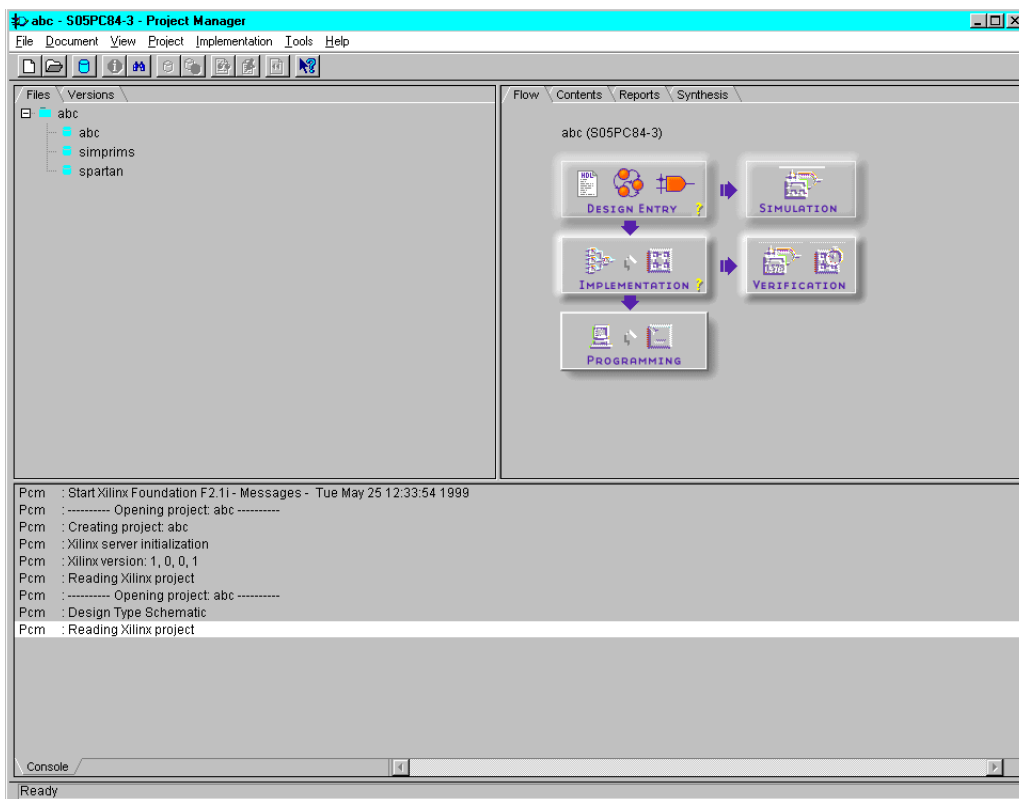


Figure 8-1 Project Manager - Schematic Flow

Extensive online help and multiple online tutorials are available from the Project Manager's Help menu. In addition, refer to the hardcopy *Foundation Series 2.1i Quick Start Guide* and *Foundation Series User Guide* included with this release for more information on using Foundation.

Multiple online books are available from the Documentation CD included with this release. Refer to the "Documentation" chapter for a list and description of the available online books and other documentation.

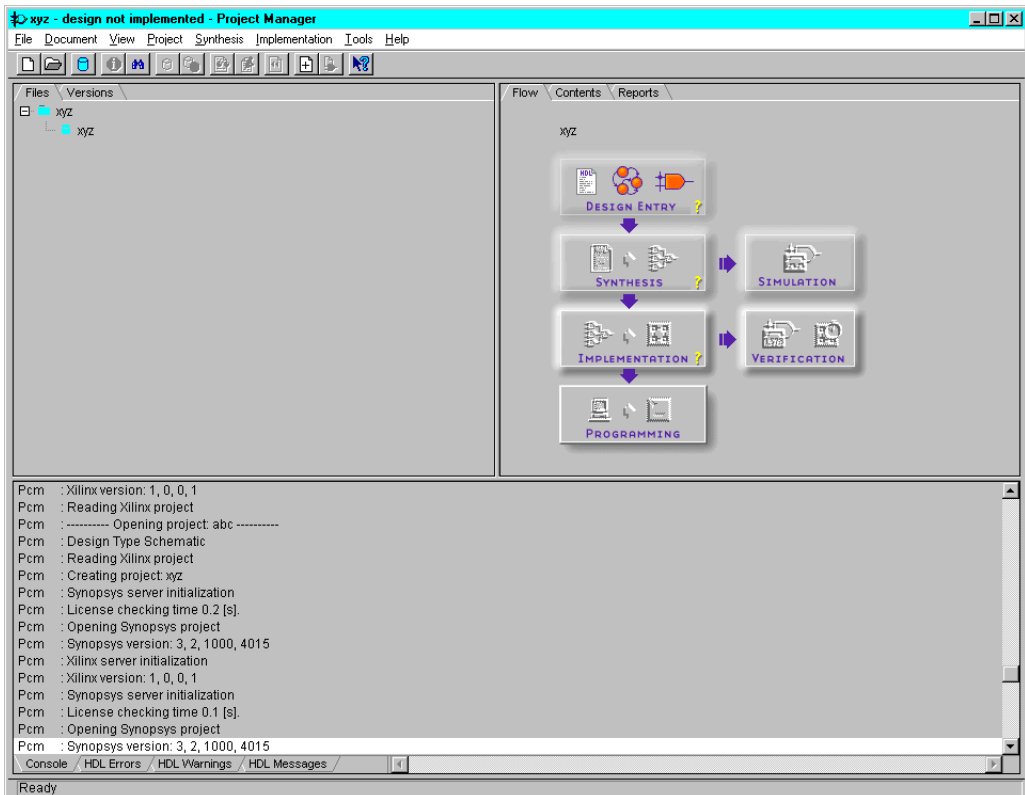


Figure 8-2 Project Manager - HDL Flow

## Using the Docsan Documentation Index

The Docsan documentation index enhances the searching capabilities of your PC's HTML browser. It works best with version 4.0 or higher of Netscape Navigator or Internet Explorer. The Netscape Navigator browser can be installed from your Design Environment CD or Documentation CD. (Refer to the "Documentation" chapter for instructions on how to install Netscape Navigator, if necessary.)

You can access the Docsan index and online book collection using any of the following methods:

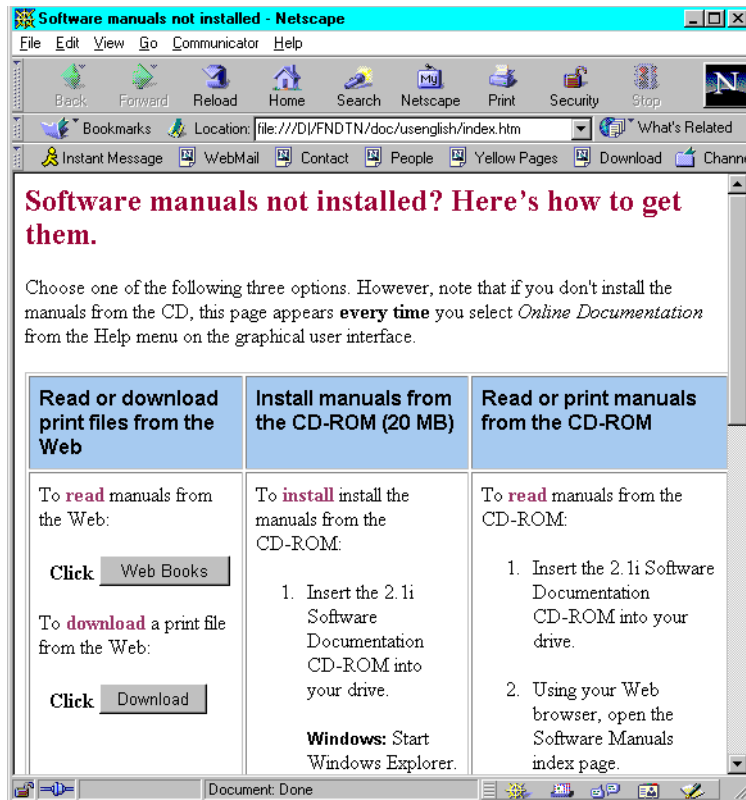
- Insert the Documentation CD into your PC's CD-ROM drive. Open Windows Explorer (or Windows NT Explorer) and double click on your CD-ROM drive. Then double click on the **index.htm** file.
- Go to the Xilinx Support web site at <http://support.xilinx.com>. Click on **Software Manuals**.
- Use the following URL to go directly to the manuals on the Xilinx Support web site: [http://support.xilinx.com/support/sw\\_manuels/2\\_1i/index.htm](http://support.xilinx.com/support/sw_manuels/2_1i/index.htm).
- Select **Start** → **Programs** → **Xilinx Foundation Series 2.1i** → **Online Documentation**. If you installed the online collection on your PC's hard drive, the Docsan index immediately appears. If you have not installed the collection, the "Software Manuals Not Installed" window appears.
- Select **Help** → **Online Documentation** from the Project Manager. If you have installed the online collection on your PC's hard drive, the Docsan index immediately appears. If you have not installed the collection, the "Software Manuals Not Installed" window appears.

### "Software Manuals Not Installed" Window

If you have not installed the books on your PC's hard drive and you attempt to access online documentation from the Project Manager's Help menu or from the **Start** → **Programs** option, the window shown below appears. This window allows you to go to the Xilinx



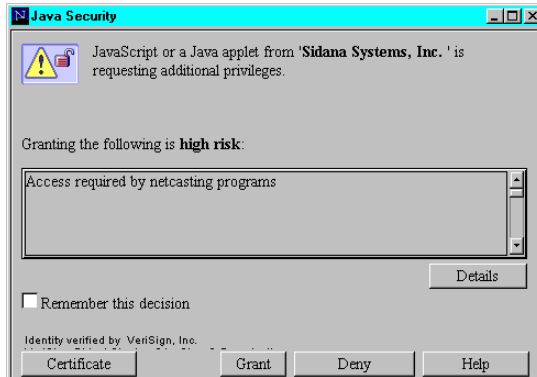
Support web site, provides information on installing the books, and instructs you on accessing the manuals on the Documentation CD.



## Docsan's Java Security

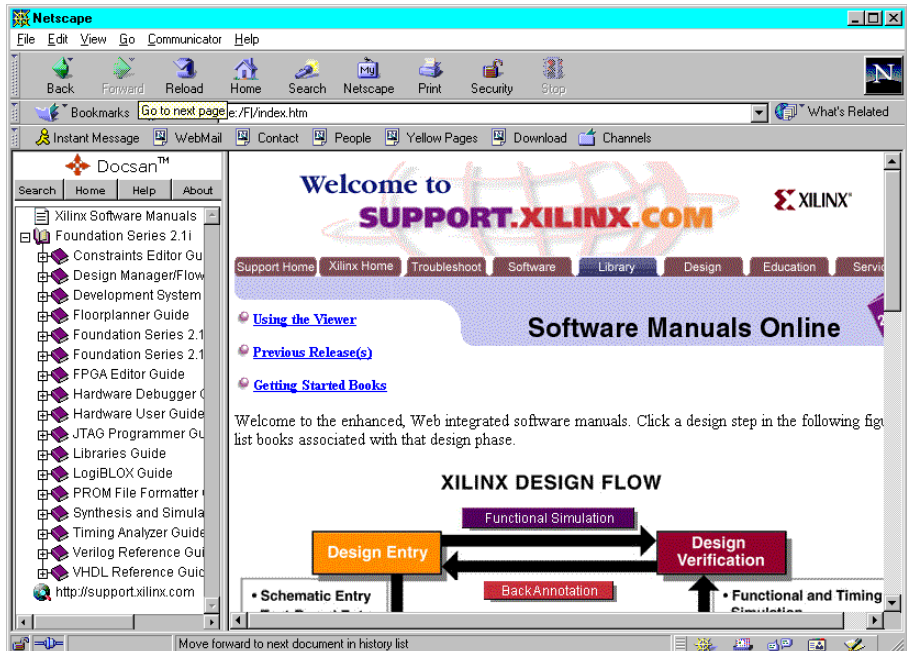
When you access the Docsan index for the first time, a "Java Security" window may appear. This window is requesting additional permissions for Docsan. For your security, the Docsan Java applet is digitally signed by Sidana Systems, Inc. using a certificate from Verisign.

Select the **Grant** or **Yes** button on the "Java Security" window to allow Docsan to access your hard drive.



## Viewing, Searching, and Printing Books in Docsan

When you access the online book collection, the main Docsan window shown below appears.



After you access the Docsan online documentation collection, use Docsan's Help function for detailed information on browsing, viewing, searching, and printing the online book collection. Basic information on these functions is included in the following subsections.

## Opening and Navigating Books

To open and view a book, do the following from the Docsan window in the left part of the screen:

1. Click the "plus" icon to the left of the Foundation Series 2.1i title to the list of books in the collection
2. Click the "plus" icon to the left of a book title to display the chapters in the book. (Continue clicking the "plus" icons under each chapter/section heading to access the sections under it.)
3. Click any chapter/section title to view the first page of the chapter/section in the right part of the screen.

## Searching the Collection

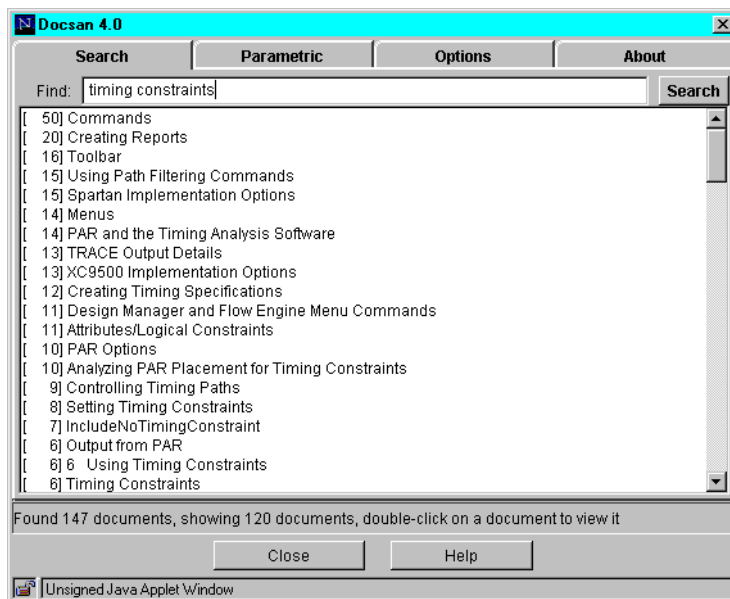
Docsan includes two types of searches. A full-text search finds every occurrence of a word or words in the book collection. A parametric search presents pulldown menu selection to focus your search. Currently, parametric searching is limited to the unified library components described in the Libraries Guide.

Click the **search** button in the Docsan window on the left of the screen to access the Search window.

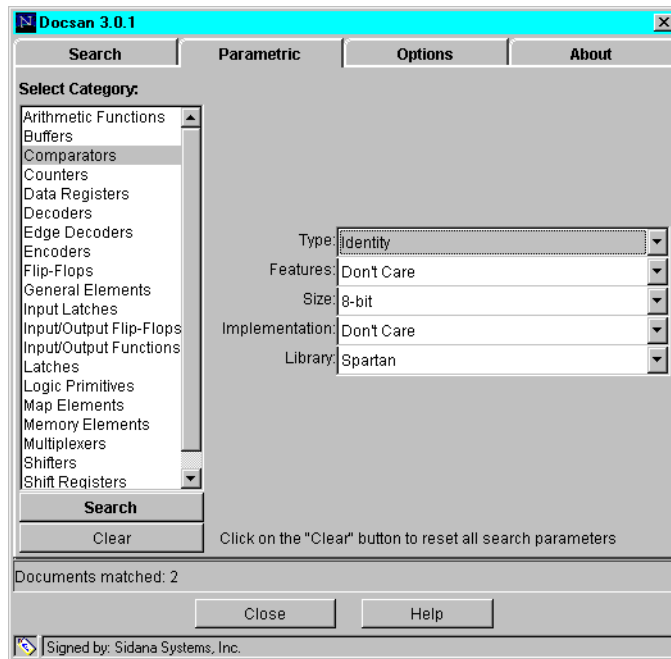
Use the tabs on the Search window to do the following:

- Initiate a full-text search

From the Search tab, enter the text string in the Find field and then click Search. The results are displayed in the results area below the Find text. Click on an item in the results area to view it.



- **Initiate a parametric search (Libraries Guide only)**  
From the Parametric tab, select a functional category (buffer, flip-flop, etc.). Select any additional criteria from the pulldown lists displayed on the right side of the Parametric search tab. The criteria available depends on the functional category chosen. Click View Results to display the list of components that match the entered criteria. Then double click on the component name to access the Libraries Guide description of that component.



- Select search options.

From the Options tab, you can select how the search results are arranged, whether you want to see the relevance rank or number of search hits, the maximum number of search results to display, etc.

## Printing a Book

Xilinx recommends that you use the PDF files for best print quality. If you do not have access to your Documentation CD, you can access the manuals in PDF format on the web and FTP each manual to your local area.

1. Insert the Documentation CD into your PC's CD-ROM drive.
2. Open your Acrobat Reader. (If you do not have Acrobat Reader installed, refer to the "Documentation" chapter for installation instructions.)
3. Select **File** → **Open** in the Acrobat Reader window.

4. Look in the “print” folder (directory) on the Documentation CD) and select the desired book. (Refer to the “Documentation” chapter for a list for online books and their PDF file names.)

# Express Software Licensing

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The use of the synthesis tools included with Base Express and Foundation Express is controlled by an Express software license.

## Who Needs an Express License?

New and existing Xilinx customers installing the Foundation Series 2.1i Base Express or Foundation Express products need a full-function, authorized Foundation Series 2.1i Express license to enable full Express functionality.

New and existing customers installing the Foundation Series 2.1i Base or Standard products do *not* need an Express software license.

## What is Express Licensing?

Base Express and Foundation Express use FLEXlm™ licenses for security. For more information about FLEXlm, see the website, <http://www.globetrotter.com>.

The FLEXlm licensing of your Express software involves the following:

- An LM\_LICENSE\_FILE environment variable set up to point to an Express license file (either the temporary Express license or the full-function Express license file)
- A temporary Express license file (typically, c:\Fndtn\data\license.dat) consisting of a license template with generic PC authorization codes and Foundation Series 2.1i package definitions
- A full-function license (typically c:\Flexlm\data\license.dat) consisting of a license template with your PC's authorization codes from Xilinx and Foundation Series 2.1i package definitions

## Temporary Express Licenses

Temporary licenses are available upon completion of a Base Express or Foundation Express installation to allow you to start designing immediately with Foundation. The temporary licenses expire in 90 days and do not authorize full functionality. The Base Express temporary license does not enable bitstream creation. The Foundation Express temporary license has the following limitations:

- The Express constraints editor and timing analyzer GUIs are not available.
- No bitstream can be created for downloading.

During installation, the setup program will attempt to install the temporary Express license (%XILINX%\data\license.dat). It will also attempt to set the LM\_LICENSE\_FILE to point to that temporary license to enable limited Express functionality. The attempts will be successful if your PC does not currently have a license.dat file or if the LM\_LICENSE\_FILE is not already defined. In this case, the temporary license is installed and setup automatically for immediate use.

If you had a license.dat file and/or if the LM\_LICENSE\_FILE variable was already set before you started the Foundation Series 2.1i Design Environment installation, the installation will not modify the existing file or variable. A message at the end of the installation will inform you of the status of its attempt to setup the temporary license. You may need to manually modify the LM\_LICENSE\_FILE to point to the temporary license file after the installation if you want to enable limited Express functionality before you get your authorized full-function license.

At the end of the installation process, be sure to watch for the screen that informs you of the status of the LM\_LICENSE\_FILE environment variable and license.dat file. If you are instructed to set the LM\_LICENSE\_FILE variable, refer to the “Setting Up the LM\_LICENSE\_FILE Variable” section for instructions.

## Full-Function Express Licenses

A Foundation 2.1 full-function license enables full Base Express or Foundation Express functionality on your PC. After you install a Foundation Series Express product you will need to either setup a



new, full-function license or modify your existing Express license to enable full Express 2.1i functionality.

## New, Full-Function Express Licenses

The following customers need to obtain and setup a new Express license after installation of the Foundation Series 2.1i product.

- New Xilinx customers installing the Base Express or Foundation Express product
- Existing Xilinx customers upgrading to Base Express or Foundation Express from the Base or Standard product
- Existing Xilinx customers upgrading to Foundation Express from the Base Express product

If you are a new Express customer, you need to do the following to obtain your full-function Express license.

- Register your software with Xilinx.
- Obtain the necessary authorization codes from Xilinx (to include in the license.dat file) for an Express full-function license.
- Ensure that you have the proper package definitions for Foundation Series 2.1i in your license.dat file.
- Ensure that the LM\_LICENSE\_FILE points to your Express license file.

Refer to the “Setting up a New, Full-Function Express License” section and the “Setting Up the LM\_LICENSE\_FILE Variable” section for details.

## Modifications to Existing Express Licenses

The following customers do not need a new Express license. They only need to modify the package definitions in their current, full-function Express licenses.

- Existing Xilinx customer updating their current Base Express product to Foundation Series 2.1i
- Existing Xilinx customers updating their current Foundation Express product to Foundation Series 2.1i

Refer to the “Modifying the Package Definition” section for details.

## Setting up a New, Full-Function Express License

Following is the procedure to setup a new, full function Express license.

### 1. Register your software.

The registration process provides your End User ID required for the Express licensing process.

On the web:

You can register online after the installation or go to <http://support.xilinx.com>. Click the Register icon in the lower left corner of the support home page to bring up the Registration screen. Enter the information requested on the screen. Then click **Submit Registration**.

By mail:

To register by mail, fill out the Xilinx registration card enclosed in your package and *fax or mail* it to your Customer Service location.

### 2. Gather the following information to use to obtain your full-function license.

- Your End User ID number

Customer Service will send you this after you register your software.

- The product name and serial number of the product you purchased

These are located in the lower right hand corner of the barcode label on the package or on the registration card inside the package.

- Your PC's Ethernet address or C drive serial number and the network name of your PC

To obtain the Ethernet address or C drive serial number, run the `lmttools.exe` application located in `c:\Fndtn\bin\nt`.

When the Lmtools window appears, click on `Hostid`.

The Hostid window of the Lmtools utility appears. Write down the following information shown in that window:

- the Ethernet address (the 12-digit number second from the bottom)
- the C: drive Volume Serial Number (the bottom number)
- the computer's network name listed in the HOSTNAME field

3. After you receive your End User ID and have gathered the other information listed in step 2, you can get the authorization codes for your full-function Express license from Customer Service. You can use any of the following methods to obtain the authorization codes.

- Use the licensing tool on the Xilinx support web site at <http://support.xilinx.com/support/license.htm>. (You must be a current Xilinx customer with a warranty registration to use this tool.)
- Complete the License Request Form enclosed in your package and FAX to the numbers listed in the "Customer Service" section of the "Software Service and Support" chapter.
- Call Customer Service. Refer to the "Customer Service" section of the "Software Service and Support" chapter for phone numbers and hours.

4. After you receive the package definitions and authorization codes, you can create your full-function Express license from the file your Xilinx Customer Service Representative sends to you.

The file your Xilinx Customer Service Representative will email or fax to you includes information similar to the following file.

#### License Information With Ethernet Address

```
#-----  
#  
# This license is nodelocked and uncounted.  
# It does NOT require or SUPPORT running lmgrd.  
#  
# Set the LM_LICENSE_FILE variable to point to this  
# license file; like:
```

```
#
# setenv LM_LICENSE_FILE=C:\xilinx\data\license.dat
# or
# set LM_LICENSE_FILE=C:\flexlm\license.dat
#
#-----
#
# This license is nodelocked to laptop,
HOSTID=00A024A9EA43
#
INCREMENT FND-EXP-PC xilinxd 1.000 29-jan-2001 0 FC93B64832A8A3DE4DAB \
"XSJ_davet" 00a024a9ea43
#
#-----
#
# Package Definitions Follow:
# These are REQUIRED for your license to work properly.
#
#-----
#
PACKAGE FND-EXP-PC xilinxd 1.000 2080B0F13916AA26C238 \
COMPONENTS="system-PC bit-PC \
xc3000D-PC xc4000X-PC xc5200X-PC \
ngd2vhdl-PC verilog-PC \
Foundation-PC X-VHDL-PC \
FPGA-Express:2000.05 \
FPGA-Express-VHDL-Base:2000.05 \
FPGA-Express-VLOG-Base:2000.05 \
FPGA-Express-XC3k-Optimizer:2000.05 \
FPGA-Express-XC4k-Optimizer:2000.05 \
FPGA-Express-XC5k-Optimizer:2000.05 \
FPGA-Express-VIRTEX-Optimizer:2000.05 \
FPGA-Express-XC9k-Optimizer:2000.05 \
FPGA-Express-Constraint-Mgr:2000.05 "
#
#
#-----
# License checksum:
#
#      82: INCREMENT FND-EXP-PC xilinxd 1.000 29-jan-2001 0
FC93B64832A8A3DE4DAB "XSJ_davet" "XSJ_davet" 00a024a9ea43
#
```

```
# (From lmutil lmcksum -c <license file>)
#
#-----+
```

If you supply a disk drive serial number, the INCREMENT line will have the text "DISK\_SERIAL\_NUM". For the previous sample file, the INCREMENT line looks like the following:

```
INCREMENT FND-EXP-PC xilinxd 1.000 1-jan-0 0 FC93B64832A8A3DE4DAB \
"XSJ_davet" DISK_SERIAL_NUM=C102011D5
```

This information in this file must appear in your license.dat file.

*Xilinx strongly recommends that you use the Ethernet address as your host id instead of the C: drive serial number.*

You can use the information you receive from Xilinx in the following ways:

- If the Customer Service Representative sent the information by email, you can remove the email header from the file and copy the file to desired location for your full-function Express license file.
- If the Customer Service Representative sent the information in a fax, you can use a text editor to create a file containing the information and place the file in the desired location for your full-function Express license file.

The default license file may contain multiple PACKAGE definitions. Most will not be relevant to your installation, but they may be left in the license file. You *must* include a package definition which corresponds to any products mentioned in INCREMENT lines. For example, the PACKAGE FND-EXP-PC line in the sample file, License Information With Ethernet Address, must be matched by an INCREMENT FND-EXP-PC line.

Each INCREMENT line must be a single line. If the text overflows to another line, use the backslash character as a continuation character at the end of the line.

If you use the backslash, make sure that it is the last character on the line. No tabs or spaces may follow the backslash.

- If you are adding the information to an existing license.dat file, place the new Xilinx information *before* any existing information pertaining to floating licensing. This information usually begins with a SERVER line.

## Setting Up the LM\_LICENSE\_FILE Variable

Your temporary license is typically located in C:\FNDTN\DATA, but Xilinx recommends not placing your full-function license file in this directory. Instead, place your full-function license file in the directory that will not be overwritten by any reinstallation of the Foundation Series software (for example C:\FLEXLM). You may have to create the directory C:\FLEXLM to place the license file in this location.

Wherever you place your full-function license.dat file, you must ensure that the LM\_LICENSE\_FILE variable points to the location of this file.

Use the procedures described in the following “Window NT 4.0” and “Windows 95/98” sections to modify the LM\_LICENSE\_FILE variable, as necessary, to point to your full-function license file.

**Note:** The procedure described below also applies to modifying the LM\_LICENSE\_FILE variable to point to the temporary Express license if you were instructed to set the LM\_LICENSE\_FILE variable after the Foundation installation.

### Windows NT 4.0

1. From the Start Menu, select the Settings folder and click on the Control Panel icon.
2. In the Control Panel, double click the System icon.
3. Select the Environment tab from the System Properties window.
4. In the Variable field, type `LM_LICENSE_FILE`.
5. In the Value field, type in the drive letter or network letter and full path of the license file. For example, for the license.dat file on the C drive located in \FNDTN\DATA, you would type the following;

```
c:\FNDTN\DATA\license.dat
```

**Note:** If you are already running FLEXlm security as part of another vendor’s software, you can set up the LM\_LICENSE\_FILE variable to point to the Xilinx license.dat file and the vendor’s license file. You can specify multiple license files in the LM\_LICENSE\_FILE Value and separate each with a semicolon (;), as in the following example.

```
c:\other_vendor\license.dat;c:\FNDTN\DATA\license.dat
```

6. Select **Set** and **Apply** to set the variable.
7. Select **OK**.
8. To verify that you set the variable, select **Start** → **Programs** → **Command Prompt**. In the Command Prompt window, enter the following command:

```
echo %LM_LICENSE_FILE%
```

The full path that you set as the value of the variable should display.

**Note:** If you do not set the LM\_LICENSE\_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the LM\_LICENSE\_FILE environment variable must be set as described previously.

**Note:** Make sure you do not have an LM\_LICENSE\_FILE variable set in the System Variables area and another one set in the User Variables area; the variable must be set in one area only.

### Windows 95/98

1. Add the following line to your autoexec.bat file.

```
set LM_LICENSE_FILE=c:\FNDTN\DATA\license.dat
```

**Note:** If you are already running FLEXlm security as part of another vendor's software, you can set up the LM\_LICENSE\_FILE variable to point to the Xilinx license.dat file and the vendor's license file. You can specify multiple license files in the LM\_LICENSE\_FILE Value and separate each with a semicolon (;), as in the following example.

```
set LM_LICENSE_FILE=c:\other_vendor\license.dat;c:\FNDTN\DATA\license.dat
```

2. Reboot your system so that the autoexec.bat file is reread. Otherwise, the change has no effect.
3. To verify that you set the variable, select **Start** → **Programs** → **MS-DOS Prompt**. In the DOS window, enter the following command:

```
echo %LM_LICENSE_FILE%
```

The full path that you set as the value of the variable should display.

**Note:** If you do not set the LM\_LICENSE\_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the LM\_LICENSE\_FILE environment variable must be set as described previously.

## Modifying the Package Definition

If you are upgrading from Base Express or from Foundation Express 1.5i (or earlier) to 2.1i, you must manually update your existing license file. To update this file, perform the following steps:

1. Locate the existing full-function Foundation license file. This file is typically located at C:\flexlm\license.dat and will have FND-BSX-PC or FND-EXP-PC increment lines similar to the following:

```
INCREMENT FND-BSX-PC xilinxd 1.000 01-JAN-0 0 CCE4DEC687D2773BB062 \
"XSJ_davet" 00a024a9ea43
```

```
INCREMENT FND-EXP-PC xilinxd 1.000 01-JAN-2002 0 EC02A904B384F4A3A07E \
"XSJ_davet" 00a024a9ea43
```

2. Open the license.dat file using a plain text editor.
3. Replace the existing PACKAGE definitions with the PACKAGE definitions shown at the end of this section.

You can either remove the existing package definition or comment it out using "#".

Copy the appropriate upgrade (FND-BSX-PC or FND-EXP-PC) PACKAGE definition shown on the following page into the license.dat file. You can find these definitions in electronic format in a file named "license\_upgrade.txt." The license\_upgrade.txt file is located on the Foundation Series 2.1i Design Environment CD and is also copied to the Foundation Series 2.1i installation area.

- Foundation Series 2.1i Design Environment CD  
Insert the CD in the CD-ROM drive (assume D:\). The package definitions are located in D:\license\_upgrade.txt.
- Foundation Series 2.1i installation area on your PC

After installing Foundation go to the area you installed it to on your PC. The package definitions are located in C:\FNDDTN\data\license\_upgrade.txt.



**Note:** The PACKAGE line must not have blanks or other white space before the keyword "PACKAGE." Also, subsequent lines must not have blanks or other white space following the backslash continuation character (\).

### For FND-BSX-PC

```
#
PACKAGE FND-BSX-PC xilinxd 1.000 E0F020D1A8C7F75BCF4A \
  COMPONENTS="system-PC bit-PC\
  xc3000D-PC xc4000E-PC xc5200E-PC \
  ngd2vhdl-PC verilog-PC \
  Foundation-PC X-VHDL-PC \
  FPGA-Express:2000.05 \
  FPGA-Express-VHDL-Base:2000.05 \
  FPGA-Express-VLOG-Base:2000.05 \
  FPGA-Express-XC3k-Optimizer:2000.05 \
  FPGA-Express-XC4k-Optimizer:2000.05 \
  FPGA-Express-XC5k-Optimizer:2000.05 \
  FPGA-Express-VIRTEX-Optimizer:2000.05 \
  FPGA-Express-XC9k-Optimizer:2000.05 "
```

### For FND-EXP-PC

```
#
PACKAGE FND-EXP-PC xilinxd 1.000 20405041295F375FE6F6 \
  COMPONENTS="system-PC bit-PC \
  xc3000D-PC xc4000X-PC xc5200X-PC \
  ngd2vhdl-PC verilog-PC \
  Foundation-PC X-VHDL-PC \
  FPGA-Express:2000.05 \
  FPGA-Express-VHDL-Base:2000.05 \
  FPGA-Express-VLOG-Base:2000.05 \
  FPGA-Express-XC3k-Optimizer:2000.05 \
  FPGA-Express-XC4k-Optimizer:2000.05 \
  FPGA-Express-XC5k-Optimizer:2000.05 \
  FPGA-Express-VIRTEX-Optimizer:2000.05 \
  FPGA-Express-XC9k-Optimizer:2000.05 \
  FPGA-Express-Constraint-Mgr:2000.05 "
  FPGA-Express-GAT:2000.05 "
```



## Uninstalling Xilinx Software

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To uninstall Xilinx Design Environment software, perform the following steps.

1. Double-click the **My Computer** icon.
2. Double-click the **Control Panel** icon.
3. Double-click the **Add/Remove Programs** icon.
4. Ensure that the **Install/Uninstall** tab is selected in the Add/Remove Programs Properties window.
5. From the list, select **Xilinx Foundation Series x** where *x* is the currently installed version of Foundation
6. Click **Add/Remove**.

When uninstalling Xilinx software, only the last install is undone. If you did multiple installs, you may need to remove some files and/or icons manually.

### PC Lab Installation (Device Download Tools Only)

The PC Lab Installation (Device Download Tools Only) does not include an uninstall program. You must delete it manually.

### Documentation CD

The Documentation CD does not include an uninstall program. The Docsan online collection is not uninstalled when the Xilinx Foundation Series *x* software is uninstalled. You must delete it manually.



## Known Issues

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This chapter describes the most critical known issues in the Foundation Series 2.1i release at press time.

**Note:** Be sure to read the “Installation” and “Online Documentation” sections of this chapter before attempting to install the Foundation Series 2.1i software tools.

For a complete, up-to-date listing of Known Issues, go to the Xilinx Technical Support Web site at <http://support.xilinx.com> and use one of the following methods.

- Look for solutions about a specific software tool

The “Technical Tips” area provides updated lists of the top and hot issues of each software release. These lists are organized by CAE tool, implementation tool, and design flow step. The following location is the Technical Tips index. Go to the following location and click the link for the tool you are using.

<http://support.xilinx.com/support/techsup/journals/index.htm>

“Technical Tips” used to be the “Expert Journals” section on the Technical Support Web site.

- Use “Answers Search” to search the Solutions Database

The advanced answers search form and a link to the Solutions Database are located at the following URL.

<http://support.xilinx.com/search/searchtd.htm>

## Installation Issues

The following known issues relate to installation.

1. VirtexE / Spartan2: Why are these families grayed out during installation / How can I enable software support for them?

Description: Both the VirtexE and Spartan2 device families require a special CD-Key to be entered during Installation in order to enable their use in the 2.1i software.

Reference: <http://support.xilinx.com/techdocs/6590.htm>

2. The first installation screen stays up for over 40 seconds, and when it disappears, nothing happens for 10 seconds.

This is a normal occurrence with this installation program; the second installation screen will appear shortly.

3. Traditional Chinese Windows machines may display unreadable characters in the “Enter User Information” installation screen.

Workaround: Make sure you use English characters to enter your user information.

4. PC systems: After installation, Design Manager may not start.

This situation is caused by a shared DLL in the system directory.  
Workaround: change your path variable settings so that `%XILINX%\bin\nt` is at the beginning of your PATH.

## Documentation and Online Help Issues

The following issues relate to Software Manuals and online help.

1. When I start the documentation viewer (index.htm) for the first time, I get a “Grant Java Permission” screen.

Click “Grant” to accept the digital certificate. This certificate is for your protection; it allows a Java program to be run on your system every time you access the Software Manuals. If you experience any problems with the documentation viewer, you can contact Sidana Systems.

2. During documentation installation, I deselected the “document viewer” option and I got an error message.

In order to view the Software Manuals online using your web browser, you need to install the documentation viewer files.

3. There is no option to install DynaText.

The Xilinx Software Manuals are now in HTML, and can be read in your web browser by installing the new Docsan documentation viewer or going directly to the Xilinx Support Web site. If you need access to older versions of Xilinx Software manuals, make sure you install the 2.1i Software tools and Documentation into a directory different than your previous software version. During installation, your old software version will be overwritten.

4. My browser window crashes when I start the documentation viewer.

Do not attempt to resize your browser window until all of the information has been loaded. Otherwise, your browser window may crash or hang. If this happens, close and then re-start your Web browser.

5. Users of Korean and Chinese Windows 95/NT systems will not have the submicron character display properly when viewing online documentation.

Workaround: Make sure you are using the localized version of Microsoft Internet Explorer 4.0 or above. You can download this application from the Microsoft Web site.

<http://www.microsoft.com>

## Design Entry Issues

The following issues relate to design entry tools.

1. Foundation 2.1i: Virtex unified library macros/primitives not supported in the HDL flow

Description: In an HDL flow project containing a top-level schematic with Virtex unified library macros or primitives, Express issues the following warning: "Cannot link cell 'M2\_1/\$1I9' to its reference design 'AND2'. (FPGA-LINK-2)."

Reference: <http://support.xilinx.com/techdocs/6987.htm>

2. Foundation 2.1i: Timing Simulation netlist always created on subsequent runs

Description: Regardless of whether the Simulation Netlist switch is set to OFF or not, a timing sim EDIF netlist is created on runs after the first revision. In the first revision if the switch is turned to OFF, it works properly and does not create the file.

Reference: <http://support.xilinx.com/techdocs/6995.htm>

3. Foundation ABEL: Internal Error 0001: assert event at line 376 in file "Z:\Lib\tsokit\TSOCELL\TSO\_SIG.C"

Description: Refer to solution 4996 for more details.

Reference: <http://support.xilinx.com/techdocs/4996.htm>

4. Foundation ABEL: ABEL2EDIF creates an incorrect netlist when the underscore character is used at the end of a signal name and gives "based:24" error in Translate

Description: Translate (EDIF2NGD) give the following warning when processing a design created in ABEL:

ERROR:based:24 - On or above line <xx> in file "<project directory>/<project>.edn": Duplicate instance, "FF\_XXXXXX", in cell "<abel file name>". This likely means that the EDIF netlist was improperly written. Please contact the vendor of the program that produced this EDIF file.

Reference: <http://support.xilinx.com/techdocs/4766.htm>

5. Foundation ABEL: Out Of Memory error or long compile times (@CARRY directive)

Description: Designs that have wide width arithmetic functions, 16-bit adders for example, may take a long time to compile or cause an Out of Memory error.

Reference: <http://support.xilinx.com/techdocs/1669.htm>

6. Foundation ABEL: Compiler does not run when installed on a network drive

Description: Refer to solution 1669 for more details.

Reference: <http://support.xilinx.com/techdocs/1669.htm>



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## Translation Issues

The following issues relate to design translation.

1. Foundation 2.1i: “The server threw an exception”

Description: When attempting to implement a design, Foundation 2.1i may display a dialog box titled "Flow Engine" with the text: "The server threw an exception." Or, the FE.LOG file may include the aforementioned text at the end its report.

Reference: <http://support.xilinx.com/techdocs/6660.htm>

2. Unisim, Simprim Simulation: DUTY\_CYCLE\_CORRECTION property on BUFGDLL in UCF file may not be seen by sim model

Description: DUTY\_CYCLE\_CORRECTION and FACTORY\_JF attributes put on BUFGDLL elements in the UCF file are not pushed down to the CLKDLL elements. The output is a bad simulation result.

Reference: <http://support.xilinx.com/techdocs/6429.htm>

3. NGDBuild: “ERROR: bascp: 94 - Invalid UCF/NCF file entry value "" detected on line 4, offset 64”

Description: When the Constraints Editor writes out constraints, it puts double quotes around all the signals. This causes a problem if the bus notation is parenthesis in the netlist.

Reference: <http://support.xilinx.com/techdocs/5054.htm>

4. Virtex NGDBuild: “ERROR: NgdHelpers: 664 - Period specification "TS\_clkdv" references the TNM group "clkdv", which contains only pad elements”

Description: NGDBuild gives errors when the TNM group contains a CLKDLL and its output drives the OBUF out to the OPAD.

Reference: <http://support.xilinx.com/techdocs/6402.htm>

5. NGDAnno 2.1i: When a block RAM has multiple input pins that are tied to ground by different nets, NGDAnno with NGM may lose one of those connections, resulting in a floating input pin. This could result in an "X" at the block RAM output.

Description: When a block RAM has multiple input pins tied to ground by different nets, NGDAnno with NGM may lose one of the connections, resulting in a floating input pin.

Reference: <http://support.xilinx.com/techdocs/6665.htm>

## FPGA Implementation Issues

The following known issues pertain to FPGA Implementation tools.

1. Foundation 2.1i: Disable guide or Floorplan does not work when selecting the option to copy using custom file

Description: When selecting the option to copy a custom guide file or Floorplan file, the switch used to enable guide/Floorplan does not work. The guide/Floorplan file is still used during implementation.

Reference: <http://support.xilinx.com/techdocs/6989.htm>

2. Foundation 2.1i: Custom guide file setting is reset for each new revision

Description: The custom guide file setting must be set for each revision. The information is not passed from one revision to the next.

Reference: <http://support.xilinx.com/techdocs/6990.htm>

3. Design Manager/Template Manager 1.5i/2.1i: How to enable Express Mode Configuration option for the SpartanXL family

Description: In order to declare Express Mode Configuration for the SpartanXL family, you must use the Template Manager Utility.

Reference: <http://support.xilinx.com/techdocs/2328.htm>

4. 2.1i Virtex MAP: Device utilization appears to increase because of new default packing rules

Description: Virtex MAP will appear to have increased device utilization in 2.1i compared to 1.5i because less unrelated packing is being done. This change actually improves routability of designs.

Reference: <http://support.xilinx.com/techdocs/6572.htm>

5. 2.1i Virtex MAP: Virtex design faults in MAP after "Removing unused logic..."  
Description: Virtex MAP may crash on designs using 5-input EQN symbols.  
Reference: <http://support.xilinx.com/techdocs/4991.htm>
6. 4KXL MAP: MAP errors out on carry logic when trimming is disabled  
Description: This problem can be avoided if unused logic trimming is not disabled.  
Reference: <http://support.xilinx.com/techdocs/5394.htm>
7. 1.5i/2.1i MAP: "FATAL\_ERROR: basnc: basncsignal.c: 263:1.67 - Could not find a bel..."  
Description: The failure is taking place during optimization and can be avoided by modifying optimization options.  
Reference: <http://support.xilinx.com/techdocs/6562.htm>
8. 1.5i/2.1i MAP: a.mfp constraint for LOC'd FF is incorrectly overridden by "-pr b"  
Description: MAP may override Floorplanner constraints if the -pr (pack registers in IOBs) option is used.  
Reference: <http://support.xilinx.com/techdocs/6563.htm>
9. 2.1i Virtex PAR: MPPR usage less effective due to less dependence on cost table differences  
Description: The Virtex placer in 2.1i is less dependent on cost table usage, so MPPR may not yield substantial differences between cost tables.  
Reference: <http://support.xilinx.com/techdocs/6573.htm>
10. 2.1i Virtex PAR: Virtex designs can not be run through guided PAR using 1.5i guide designs  
Description: Version 2.1i introduced a new mapping algorithm for Virtex devices. Mapping results will vary significantly from 1.5i designs so that the 1.5i designs are unusable as guide designs in 2.1i. PAR will accept the 1.5i designs as input, but results will be very poor.

Reference: <http://support.xilinx.com/techdocs/6574.htm>

11. 2.1i Virtex PAR: Virtex placer may crash when placing routed hard macros

Description: The problem can be worked around by removing routing information from Virtex hard macros.

Reference: <http://support.xilinx.com/techdocs/6568.htm>

12. 1.5i/2.1i Virtex PAR: PAR crashes with “Exception: access violation (0xC0000005) Address 0x031335A6”

Description: This crash occurs when a standard IOB component is LOC'd to a GCLKIOB site. There is a related MAP issue where BUFGs will be mapped to standard IOBs unless an IBUFG is inserted between the PAD and BUFG.

Reference: <http://support.xilinx.com/techdocs/6408.htm>

13. 4KXL PAR: 4036XL design unable to place some CLBs clocked by BUFG

Description: The work around is to replace the BUFGs with BUFGS's.

Reference: <http://support.xilinx.com/techdocs/5704.htm>

14. FPGA Editor: FPGA Editor adds incorrect file extension when saving designs as macros

Description: Refer to solution 6197 for details on how to specify the correct file extension.

Reference: <http://support.xilinx.com/techdocs/6197.htm>

15. FPGA Editor: FPGA Editor displays edge decoders for Spartan and SpartanXL devices

Description: Wide edge decoders are not supported in Spartan and SpartanXL devices and should not be displayed.

Reference: <http://support.xilinx.com/techdocs/5637.htm>

16. FPGA Editor: IOB components added for probing signals are not sorted in the list window

Description: This is the result of adding the components after the LIST window has been sorted.

Reference: <http://support.xilinx.com/techdocs/6440.htm>

17. Floorplanner: Floorplanner allows illegal BUFG placement  
Description: The Floorplanner DRC does not verify the BUFG placement. The user must verify the validity of the BUFG placement.  
Reference: <http://support.xilinx.com/techdocs/6510.htm>
18. Floorplanner: Floorplanner allows illegal IBUFG placement  
Description: The Floorplanner DRC does not verify the IBUFG placement. The user must verify the validity of the IBUFG placement.  
Reference: <http://support.xilinx.com/techdocs/6164.htm>
19. Floorplanner: Floorplanner allows illegal dedicated clk pad placements  
Description: The Floorplanner DRC does not verify the clk pad placement. The user must verify the validity of the clk pad placement.  
Reference: <http://support.xilinx.com/techdocs/6359.htm>
20. Floorplanner: The Shortcuts for Select Loads, Select Source, Zoom to Box, Zoom to Part, and Expand/Collapse Hierarchy do not work  
Description: Refer to solution 6159 for more details.  
Reference: <http://support.xilinx.com/techdocs/6159.htm>

## CPLD Implementation Issues

The following issues pertain to CPLD Implementation tools.

1. 9500/XL Fitter/HITOP: PROHIBIT property does not exclude pins from "Programmable Ground Pins" option  
Description: The PROHIBIT property can be used to reserve specific device pins so they remain unused by the CPLD fitter. However, if you enable the implementation option "Create Programmable Ground Pins on Unused I/O," all unused pins, including those listed in the PROHIBIT property, are connected to the device's ground network.  
Reference: <http://support.xilinx.com/techdocs/4100.htm>

2. **ChipViewer: Scrollbar missing from chip view**

Description: For large CPLD devices 95288/XL and 95216, the scrollbar is missing. This prevents complete access to all function blocks and macrocells.

Reference: <http://support.xilinx.com/techdocs/6638.htm>
3. **ChipViewer: Input paths are not shown on input pins**

Description: The input path is not shown when you click on a input pin in the ChipViewer.

Reference: <http://support.xilinx.com/techdocs/6639.htm>
4. **CPLD Fitter: Test Vectors targeting a 9500/XL/XV CS48 and BG352 package**

Description: When using Test Vectors with a 9500/XL/XV CS48 or BG352 package, the JTAG Programmer functional test may give erroneous results. The JEDEC file will program the design correctly, the problem is strictly with the test vectors.

Reference: <http://support.xilinx.com/techdocs/6647.htm>
5. **CPLD Fitter 2.1i: Access violation error when using a test vector file for xc95288xl BG256**

Description: When using test vectors with a 9500XL/XV BG256 package a core dump will appear at the hprep6 stage. The only workaround for this package is to produce a JEDEC file without test vectors.

Reference: <http://support.xilinx.com/techdocs/6645.htm>
6. **CPLD Fitter: Attributes ignored when using the Constraints Editor and quotes are placed around signal qualifier**

Description: When using the Constraints Editor some attributes have quotes added around the signal qualifier which the CPLD Fitter does not recognize.

Reference: <http://support.xilinx.com/techdocs/6640.htm>
7. **Timing Analyzer Engine: Empty report file**

Description: When running the Timing Analyzer, the editor will default to showing an empty report file if the detailed report exceeds 2,000,000 paths.

Reference: <http://support.xilinx.com/techdocs/5111.htm>

8. CPLD Fitter: OFFSET timespec is not supported

Description: The OFFSET attribute is N/A in CPLD designs. It is not supported in this version of the software.

Reference: <http://support.xilinx.com/techdocs/5999.htm>

## Functional and Timing Simulation Issues

The following issues pertain to the design steps of functional and timing simulation.

1. Foundation 2.1i: Checkpoint Gate Simulation Control issues error when selecting NGD file

Description: If you select the checkpoint simulation menu option and then select a netlist (e.g. <project>.ngd), a dialog pops up saying "Unknown error <OK>."

Reference: <http://support.xilinx.com/techdocs/7005.htm>

2. Foundation Simulation: Timing Simulation of Virtex DLL (CLKDV\_DIVIDE)

Description: The CLKDV\_DIVIDE value is not applied during Timing Simulation. The attribute is applied to the physical design; however, it is ignored during timing simulation.

Reference: <http://support.xilinx.com/techdocs/6966.htm>

## Timing & Constraints Issues

The following known issues relate to timing and constraints.

1. ERROR: basut: 162: This Xilinx application has run out of memory or has encountered a memory conflict

Description: This error is the result of insufficient RAM or large device sizes. This issue is currently under investigation.

Reference: <http://support.xilinx.com/techdocs/6445.htm>

2. TRACE/Timing Analyzer: Phase on Virtex DLL taps not accounted for in timing analysis

Description: Refer to solution 2586 for information on accounting for phase in your constraints.

Reference: <http://support.xilinx.com/techdocs/2586.htm>

3. TRACE/Timing Analyzer: Skew not automatically accounted for on Virtex Low skew clocks

Description: Refer to solution 6449 for details on reporting skew during PAR and TRACE.

Reference: <http://support.xilinx.com/techdocs/6449.htm>

4. TRACE/Timing Analyzer: Unconstrained path report contains constrained paths

Description: The unconstrained path report contains the constrained paths first, then the unconstrained paths.

Reference: <http://support.xilinx.com/techdocs/6447.htm>

5. TRACE/Timing Analyzer: Does not provide the ability to constrain the block RAM halves separately

Description: Any grouping constraints applied to either half of a block RAM, results in the group being applied to both halves. This issue is currently being addressed.

Reference: <http://support.xilinx.com/techdocs/6448.htm>

6. Timing Analyzer: Block RAM components are not listed in RAM Sources/Destinations element types

Description: This issue is currently being addressed.

Reference: <http://support.xilinx.com/techdocs/6245.htm>

7. Constraints Editor: The pad group pulldown list in the Clock to Pad and Pad to Setup dialog, contains all groups instead of just pad groups

Description: The user must verify the group specified as a pad group.

Reference: <http://support.xilinx.com/techdocs/6380.htm>

8. Constraints Editor: TIMESPEC TSxx = FROM(abc) TO(xyz) is incorrectly translated

Description: The Constraints Editor does not understand a predefined timegroup inside of a timespec.

Reference: <http://support.xilinx.com/techdocs/6383.htm>



9. Constraints Editor: Wildcard symbol "\*" is not supported by CE  
Description: The user must explicitly tell the Constraints Editor which elements are to be used in order to apply the group in the editor.  
Reference: <http://support.xilinx.com/techdocs/6384.htm>
10. Constraints Editor: Creating relative FROM PADS TO PADS constraint in the FROM/THRU/TO dialog creates incorrect constraint  
Description: The constraint is created as an explicit constraint instead of a relative constraint.  
Reference: <http://support.xilinx.com/techdocs/6386.htm>
11. Constraints Editor: PULLUP/PULLDOWN constraints from the NGD file are not displayed  
Description: This issue is currently being addressed. Refer to solution 6355 for details.  
Reference: <http://support.xilinx.com/techdocs/6355.htm>
12. Constraints Editor: Can't override TSid from a source constraint  
Description: The Constraints Editor does not allow the user to create a TIMESPEC with an existing TSID.  
Reference: <http://support.xilinx.com/techdocs/6388.htm>

## Downloading and Configuration Issues

The following known issues relate to downloading and configuring designs.

1. Hardware Debugger 2.1i: Debugging (Capture) features for MultiLINX not Supported  
Description: Hardware Debugger 2.1i does not support debugging (Readback Capture) features through the MultiLINX cable. Currently, the only cable that is supported for debugging is the XChecker cable.  
Reference: <http://support.xilinx.com/techdocs/6549.htm>
2. Hardware Debugger 2.1i: Parallel Cable III clears target FPGA configuration after download

Description: On some PCs, after downloading with the Parallel Cable IIII, a glitch will cause the PROG lead to pulse Low thus clearing the configuration memory of the target FPGA. The Hardware Debugger will indicate that the device is successfully configured, but DONE will be Low on the target FPGA.

To fix this problem the following environment variable must be set.

```
SET XIL_HWD_PCAB_FIX=1
```

Reference: <http://support.xilinx.com/techdocs/6545.htm>

3. Hardware Debugger 2.1i: Verify SpartanXL fails with mismatches

Description: The Hardware Debugger 2.1 currently cannot successfully verify a SpartanXL device. Download works and target functions correctly, but verify will fail with varying number of mismatches.

Reference: <http://support.xilinx.com/techdocs/6558.htm>

4. Hardware Debugger 2.1i: Power loss to MultiLINX cable during download may crash application

Description: If the power supply to the MultiLINX cable is removed while a download is in progress, the Hardware Debugger may crash or freeze.

Reference: <http://support.xilinx.com/techdocs/6550.htm>

5. Hardware Debugger 2.1i: The MultiLINX USB Interface only supported for W95c/W98

Description: The MultiLINX cable supports both RS232 and USB Host connections. The Hardware Debugger will support the RS232 connection for all supported PC platforms, but only supports USB for Windows 95c and Windows 98.

Reference: <http://support.xilinx.com/techdocs/6552.htm>

6. Hardware Debugger 2.1i: Changing baud rate resets the MultiLINX cable

Description: When the MultiLINX cable is reset, the default firmware and onboard FPGA design are internally reloaded. The Hardware Debugger must download new firmware and onboard FPGA design to perform certain operations. Changing the baud rate after communication is established resets the cable requiring

the user to wait while the software reloads the needed firmware and onboard FPGA design for the desired functions.

Reference: <http://support.xilinx.com/techdocs/6553.htm>

## CORE Generator and IP Modules Issues

The following issues pertain to the CORE Generator tools and IP Modules.

1. V2.1i COREGEN: CORE Generator web links do not use the web browser specified during 2.1i installation

Description: Refer to Solution 6497 for details on how to specify your preferred Web using the `coregen_<user_name>.prf` file.

Reference: <http://support.xilinx.com/techdocs/6497.htm>

2. V2.1i COREGEN: CORE Generator GUI windows may not refresh or may simply hang on Windows NT if left running for extended periods of time

Description: The problem is currently under investigation. Please quit the CORE Generator system and then restart it.

Reference: <http://support.xilinx.com/techdocs/6149.htm>

3. V2.1i COREGEN: Windows NT, 95, 98: Cannot start up the CORE Generator system—the application hangs after loading `SizeRequirements.class`

Description: This problem is due to a conflict with a "JavaHome" setting in the Windows registry.

Reference: <http://support.xilinx.com/techdocs/6366.htm>

4. V2.1i COREGEN: The CORE Generator system ties up 15-20% of CPU when idle

Short Description: You must quit and restart the CORE Generator tool if you come across this problem.

Reference: <http://support.xilinx.com/techdocs/6242.htm>

5. V2.1 COREGEN, Foundation: Virtex block RAM generated by the CORE Generator system does not simulate initial values properly

Short Description: Zeros appear at the output instead of the initial values specified in the COE file. To work around this

problem, run the design through Translate in the Design Manager, then run a Checkpoint Gate level Simulation from the Foundation Project Manager.

Reference: <http://support.xilinx.com/techdocs/6527.htm>

## Boundary Scan/JTAG Issues

The following issues relate to Boundary Scan and JTAG functionality.

1. JTAG Programmer: Reconfiguration of a Virtex device does not perform a shut-down sequence

Description: When programming a Virtex device using the JTAG Programmer, the shut-down sequence that goes through and clears the configuration memory is not performed. This only applies to reconfiguring the device. When performing a reconfiguration, it is recommended to pulse the program pin.

Reference: <http://support.xilinx.com/techdocs/5848.htm>

2. JTAG Programmer: Chain initialization for FPGAs gives incorrect information

Description: FPGA chain initialization for those devices with an IDCODE comes up with an incorrect description.

Reference: <http://support.xilinx.com/techdocs/6643.htm>

3. JTAG Programmer: Parsing incorrect on the 4005XL TQ144 BSDL file

Description: When targeting a 4005XL TQ144 it comes up with an error that it could not find the BSDL file. A modification to the BSDL file is required that is described in the reference.

Reference: <http://support.xilinx.com/techdocs/4875.htm>

4. JTAG Programmer: Verification of FPGAs gives an error

Description: The Verify option in the JTAG Programmer for the FPGA devices is not functional. It gives warnings that there were too many mismatches when the device has been programmed correctly.

Reference: <http://support.xilinx.com/techdocs/4865.htm>

5. JTAG Programmer: LPT2 Parallel port

Description: JTAG Programmer supports the LPT1 and LPT2. When connecting to the LPT2, however, the label states connection was established for LPT1. This is an error with the labeling.

Reference: <http://support.xilinx.com/techdocs/6644.htm>



## Software Service and Support

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This chapter details how to contact Xilinx for Customer and Technical Support and how to find the most up-to-date information about Xilinx products. The following sections are in this chapter.

- “Customer Education”
- “Customer Service”
- “Searching for Answers”
- “Technical Support”

### Customer Education

Xilinx provides extensive customer training courses for all of the software product lines.

For more information about customer education and software training for Xilinx products, please refer to the Xilinx web site at <http://support.xilinx.com>

You can also contact a Xilinx Training Administrator at the following toll-free number.

**(1-877-XLX-CLASS)**

International customers please contact your local sales representative or distributor for area-specific training programs.

## Customer Service

For software licensing information, warranty status, shipping, and order management issues, contact Xilinx Customer Service using the information in the following table.

Country	Telephone	Facsimile
United States and Canada <sup>1</sup>	1-800-624-4782	408-559-0115
United Kingdom <sup>2</sup>	01932-333550	01932-828521
Belgium <sup>2</sup>	0800 73738	
France <sup>2</sup>	0800 918333	
Germany <sup>2</sup>	0130 816027	
Italy <sup>2</sup>	1677 90403	
Netherlands <sup>2</sup>	0800 0221079	
Other European Locations <sup>2</sup>	(44) 1932-333550	(44) 1932-828521
Japan	81 3 3297 9153	81 3 3297 9189

<sup>1</sup>Mon-Fri, 8:00 am - 5:00 pm Pacific time

<sup>2</sup>Monday–Friday, 9:00 a.m. to 5:30 p.m. United Kingdom time—English speaking only.

If you are an international customer, contact your local sales representative for customer service issues. Refer to the Xilinx web site at [http://support.xilinx.com/company/sales/int\\_reps.htm](http://support.xilinx.com/company/sales/int_reps.htm) for contact information.

A complete list of Xilinx worldwide sales offices is at <http://support.xilinx.com/company/sales/offices.htm>.



## Searching for Answers

The most up-to-date information about Xilinx products is found in the following areas.

### Device-Specific Information

Consult *The Programmable Logic Data Book* for device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging. *The Programmable Logic Data Book* is available in hard copy and on the Xilinx web site (<http://support.xilinx.com>). See <http://support.xilinx.com/partinfo/databook.htm> for the current version of this book.

### Design Issues and Techniques

For specific design issues or problems, use the Answers Search function on the Web (<http://support.xilinx.com/support/searchtd.htm>) to access the following.

- Answers Search: current listing of solution records for the Xilinx software tools
- Application Notes: descriptions of device-specific design techniques and approaches
- Data Sheets: pages from *The Programmable Logic Data Book*
- XCell Journal: quarterly journal for Xilinx programmable logic users
- Technical Tips (formerly known as Expert Journals): the latest news, design tips, and patch information on the Xilinx design environment

If you cannot access the Web, you can install and access the Answers book with the DynaText online browser in the same manner as the Xilinx book collection. The Answers book includes information in the Answers Database at the time of this release.

## Technical Support

The following section details how to reach the Xilinx Application Service centers for your area. If you experience problems with the installation or operation of your software, Xilinx suggests that you first go to our <http://support.xilinx.com> web site. The Xilinx technical support web site also provides forms for easily submitting your technical question by e-mail. To access these forms, go to the “Services” area of the [support.xilinx.com](http://support.xilinx.com) and click the “Open New Case” link.

You can also contact the Xilinx Technical Support hotline by phone or fax. When faxing inquiries, provide your complete name, company name, and phone number. The following table gives Worldwide contact information for Xilinx Application Service centers.

Location	Telephone	Facsimile (Fax)
North America	1-408-879-5199 1-800-255-7778	1-408-879-4442
United Kingdom	44-1932-820821	44-1932-828522
France	33-1-3463-0100	33-1-3463-0959
Germany	49-89-93088-130	49-89-93088-188
Japan	local distributor	local distributor
Korea	local distributor	local distributor
Hong Kong	local distributor	local distributor
Taiwan	local distributor	local distributor
Corporate Switchboard	1-408-559-7778	

## XABEL PLUSASM Flow For CPLD Designs

---

If you have an existing ABEL CPLD design that contains XEPLD PROPERTY (or PLUSASM PROPERTY) statements, you must either replace these properties with the supported EDIF-compatible XILINX PROPERTY statements described in the Foundation Online Help System or you must enable the PLUSASM flow as described below. If your existing design does not contain PLUSASM based properties, you should be able to use the standard EDIF-based flow described in the user documentation without modification to your design. If you are developing a new ABEL CPLD design, *do not use PLUSASM based properties*.

**Note:** PLUSASM language will no longer be accepted for design entry in later releases of Xilinx design implementation software.

The PLUSASM flow is supported only for top-level ABEL CPLD designs. If you have an ABEL module used in a schematic-based design, you must replace any PLUSASM based properties with EDIF-compatible properties and use the standard EDIF-based flow.

To enable the PLUSASM flow for ABEL CPLD designs containing PLUSASM properties, use the following procedure:

1. In the Foundation Project Manager, select **File** → **Preferences** → **Configuration**.
2. In the Configuration window, click on "View Ini File".
3. In the Report Browser window that appears, find the lines containing

```
[ EXTENSIONS ]  
;XABELNETLIST=PLUSASM
```

4. Delete the semicolon (;) in front of XABELNETLIST to enable the feature.
5. Save the file (**File** → **save**) and close the Report Browser window.
6. Click OK in the Configuration window to close it.
7. Exit the Foundation Project Manager (**File** → **Exit**) and restart it.

After the PLUSASM flow is enabled, the Foundation system creates PLUSASM formatted .PLD files for all top-level ABEL CPLD designs and the CPLD fitter software uses the .PLD files for implementation instead of EDIF netlists. FPGA designs and all ABEL macros used in schematic-based designs will continue to use EDIF netlists for implementation.

**Note:** The Foundation system continues to create EDIF netlist files in addition to the .PLD files for simulation purposes. But only the .PLD files will be used for design implementation.

To disable the PLUSASM flow and resume using the standard EDIF based flow, replace the semicolon (;) in front of the XABELNETLIST keyword in the INI file and restart the Foundation Project Manager. If you have already run your design using the PLUSASM flow and wish to rerun the same design using the standard EDIF based flow, you must create a new project and copy your design files. Otherwise, the implementation software will continue to use the existing .PLD file instead of the new EDIF netlist.

For more information in using the PLUSASM flow, refer to Solution #2776 in the Answers Database at <http://support.xilinx.com>.

## Troubleshooting

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This appendix describes possible errors or problems you might have when installing the software on personal computers.

### Installation

This section describes installation errors.

#### Insufficient Space for the Installation

The Setup program indicates if sufficient space is not available. If this error occurs, then you need to increase your disk space or install the core executables and a limited set of the remaining software.

Certain conditions may cause the Setup program to issue an erroneous insufficient space for the installation warning. If any of the following conditions apply, you can continue with the installation without increasing your disk space or limiting the items to be installed:

- When you are upgrading from one Xilinx release to another, the calculated required disk space for the install is *replacement* space for all or part of the disk space used by the currently installed version—not additional space. For example, if the install screen shows 140 MB required for the newly selected install items but the disk has only 100 MB available disk space, you receive a warning. However, the program is not taking into account the disk space occupied by the current release (for example, 130 MB) that the new install replaces. Therefore, in this example, only 10 MB is actually required for the install. You can continue with the install.
- If you do a network installation (new install or upgrade) to some Unix network drives, the Setup program may report that no disk

space is available when in fact there is plenty space available. You can continue with the install.

- You may also see negative required disk space numbers. This is due to a limitation in the install program's ability to detect/calculate available space on very large disk drives. You can continue with the install.

## Program Icons Were Not Created By Setup

If the Xilinx Setup program did not create a program group for your Windows tools and program icons for each individual tool, use the following instructions to create program groups and icons for products you have installed. The following procedure applies to both Windows 95 and Windows NT 4.0.

1. To create a new program folder, click the right mouse button on **Start**. Select **Open**.
2. After the C:\WINDOWS\Start window displays, select **File** → **New** → **Folder**. A new folder displays in the window.
3. Type a name for the new folder and press Return.
4. With the new folder selected, click **File** → **New** → **Shortcut**. The Create Shortcut window displays.
5. From the "Program Paths" table, select the path corresponding to the shortcut you want to create. The table assumes the software is installed in c:\fndtn.

**Table B-1 Program Paths**

Program Description	Path	Working Directory
Design Manager	c:\fndtn\bin\nt\dsgnmgr.exe	drive:\xilinx_user
Timing Analyzer	c:\fndtn\bin\nt\timingan.exe	drive:\xilinx_user
Hardware Debugger	c:\fndtn\bin\nt\hwdebugr.exe	drive:\xilinx_user
PROM File Formatter	c:\fndtn\bin\nt\promfmtr.exe	drive:\xilinx_user

6. Click Next. When the Select a Title for the Program window displays, enter a name for the shortcut and click Finish.
7. When the Select an Icon window displays, select one of the icons and click Finish.

8. In the C:\WINDOWS\Start window, drag the new shortcut icon into the new program folder.
9. Move the new folder containing the shortcut into the main Program folder.

## Peripherals

The following subsections describe peripheral problems that can occur.

### Mouse Is Incompatible

If your mouse is incompatible with the installation program, use the keyboard commands listed in the following table to navigate and select objects on the screen.

**Table B-2 List of Keyboard Commands**

<b>Key</b>	<b>Action</b>
Tab	Traverse objects forward and highlight them
Shift-Tab	Traverse objects backward
Enter	Activate selection button or highlighted list item, including menu items Highlight list item
Arrow keys	Scroll up or down inside selection boxes, including menus
Alt-Character	Select menu
Esc	Unselect menu Exit Help window

## Mouse Fails

The following covers possible solutions for failures you might have with your mouse.

- Your installation program does not have a built-in mouse driver. Make sure the mouse driver that you are using is compatible with Windows 95 or Windows NT.
- If you do not have a Windows-compatible mouse, refer to the “List of Keyboard Commands” table for information on how to enter commands from the keyboard.

## Licensing

The followings subsections describe licensing problems.

### LM\_LICENSE\_FILE

If you see messages indicating you are having problems getting a license, check the value of LM\_LICENSE\_FILE. The environment variable LM\_LICENSE\_FILE should point to the permanent license file at `c:\flexlm\license.dat`. If you have an evaluation license, the LM\_LICENSE\_FILE variable should point to `%XILINX\data\license.dat`.

### License Validity

Some Xilinx licenses, for example evaluation licenses, are designed to expire at a certain time. If your license has expired, you must call your Xilinx customer service representative to obtain valid license and authorization codes to place in the license.dat file. The phone numbers to use to contact your customer service representative are listed in the “Express Software Licensing” chapter.

## Design Entry Tools

For Foundation 1.4, the SUSIE.INI file is where the design entry tools store their configuration information; it resides in the `c:\windows` directory. If you are experiencing problems with the design entry tools not initializing correctly, make sure this file exists and has not been corrupted.



By default, some options are disabled from the menus, but can be enabled by editing SUSIE.INI. These options include:

- design export to XVHDL

```
[extensions]
```

```
ExportVHDL=On
```

- XACTstep 6.x flow

```
[Flow_26]
```

```
XILINX6=On
```

## Design Implementation Tools

Many problems running software result from problems in your environment. When using Xilinx products, you need to make sure that your environment (your path) is pointing to the correct sets of libraries.

### PATH Environment Variable

The PATH variable sets the overall executable search path.

### XILINX Environment Variable

The XILINX variable is used by Foundation to locate data files. It must specify the directory where the Foundation design implementation software resides. This variable is automatically set up during installation.

### Registry Entries

When the Foundation software is installed, several entries are made to the Windows NT Registry by the install program.

For Windows 95, the global environment variable, XILINX, and the path to the bin\nt directory are added to the autoexec.bat file instead of the Registry.



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