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Introducing Xilinx and Programmable Logic Solutions for Home Networking

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Summary

Xilinx has been successful in the communications and networking markets because of the dynamics in these markets. With evolving standards and specifications, the need for programmable logic solutions is being further enhanced. The consumer market is seeing a recent flux of digital convergence.

The coming of broadband access, the Internet, multiple PCs, and other information appliances is bringing applications such as streaming video, MP3 files, etc. to the homes of the consumer. Xilinx Spartan™-II FPGAs, with their high-densities, performance features, and low cost, help reduce the customer's time needed to build products. With the Xilinx Online solution, FPGAs can be reprogrammed with the updated specifications.

The eSP: Home Networking program helps system designers and ASIC/FPGA designers understand the technology and market dynamics to make the right decisions in this marketplace.

Xilinx Corporate Information

Xilinx is the leading provider of complete and innovative programmable logic solutions. The company's products help minimize risks for manufacturers of electronic equipment by reducing the time required to develop products and to take them to market. Customers can design and verify their proprietary circuits with Xilinx programmable logic devices (PLDs) much faster than they could by using traditional methods, such as mask-programmed gate arrays, application specific integrated circuits (ASICs) and application specific standard products (ASSPs). Moreover, because Xilinx devices are standard parts (they only need to be programmed), customers are not required to wait for prototypes or pay large non-recurring engineering (NRE) costs. Customers incorporate Xilinx PLDs into products for a wide range of markets, including data processing, telecommunications, networking, consumer electronics, industrial control, instrumentation, automotive, military, and aerospace.

Founded in 1984, Xilinx pioneered the field programmable gate array (FPGA), and today provides more than half of the worldwide demand for field-programmable devices. Xilinx is a publicly traded company (NASDAQ: XLNX) headquartered in San Jose, California, and employs approximately 2,300 people worldwide. Market research firm Dataquest-GartnerGroup currently ranks Xilinx as the fifth-largest application specific integrated circuit supplier in the world.

The Xilinx strategy is to provide off-the-shelf integrated circuits (ICs), software design tools, predefined system level functions such as Intellectual Property (IP) cores, Internet Reconfigurable Logic (IRL™) solutions, and unparalleled field engineering support. Xilinx helps its customers by introducing innovative products that allow customers to reduce their time-to-market and increase the time-in-market in today's dynamic marketplace. Xilinx capitalizes on its key strengths:

- Research and development (R&D), marketing and applications engineering
- Leading edge IC design and process technology
- Obtaining wafer capacity at competitive prices to produce the fastest, lowest cost, and most dense parts

Xilinx products address a broad application base, with no one customer representing more than ten percent of the company's total revenues. Xilinx products are designed primarily into the communications/networking sector with 70 percent of the revenues generated from infrastructure/cellular base stations, network routers, and switches for wide area networks (WAN) and local area networks (LAN), and wireless communication applications. Other sales

venues include computing (computer peripherals, mass storage, high-speed servers) and consumer electronics.

Operations

As a "fabless" manufacturer, Xilinx partners with leading semiconductor manufacturers—The UMC Group in Taiwan and Seiko Epson in Japan—through close business relationships or equity positions in their factories. This strategy allows Xilinx to focus on designing new product architectures, software tools, and IP cores while having access to the most advanced semiconductor process technologies. Today, Xilinx is producing PLDs using state-of-the-art 0.18- and 0.25-micron process technology, with advanced copper interconnect. Xilinx has manufacturing operations in San Jose and near Dublin, Ireland, where product design, software development, final testing, and quality analysis take place. Xilinx also has facilities in Boulder, Colorado, where much of the company's software development takes place, and in Albuquerque, New Mexico, where CoolRunner CPLDs are developed.

Products

Xilinx builds programmable logic ICs and develops software and cores providing complete solutions. Xilinx designs, develops, and markets the following products to target applications such as the consumer, wireless, embedded, networking, and telecom markets. Xilinx also provides application support and design services to help customers with their unique designs. However, each family of products has a unique focus:

- **Virtex™ series of FPGAs:** High-performance, high-density FPGAs
- **Spartan series of FPGAs:** High-volume, low-cost FPGAs
- **CoolRunner™ and XC9500XL™ CPLD families:** Low-power, low-cost CPLDs
- **Software and IP products:** Software solutions, design tools, and IP cores
- **Internet Configurable Logic (IRL):** Field upgradeability using the Internet

Programmable Logic Devices (PLDs)

In a PLD, the software is used to decide how to connect groups of transistors (gates) or groups of gates (macrocells) together in a particular way. PLDs are programmed in one of three ways:

- Connections between gates are linked by physically breaking some lines (fuses)
- Alternatively, connections are made by melting some lines (anti-fuses)
- The third method connects the gates by using software-controlled switches within the PLD

Once the connections have been made, the PLD behaves as if it were a custom-designed circuit, and one can make a generic PLD do specific things. Another way of making a customized chip (ASIC) is to have the chip designed from the beginning with fixed connections, or to have a chip that mixes groups of previously designed sections of a chip, all connected with fixed wires. The differences between PLDs and ASICs include the following:

- ASICs take much longer to be designed and manufactured (over 8-9 months). Comparatively, a PLD obtained from a distributor can be programmed instantly.
- ASICs sometimes have better performance because an ASIC design is optimized for a specific function. Conversely, PLDs have a lot more flexibility, which is important in prototyping and in early stages of design. With the migration to advanced process technologies, the cost of PLD solutions have become comparative to ASICs, and PLDs are hence winning high-volume designs.
- An ASIC has more up-front NRE costs in design and in some of the one-time manufacturing costs, like buying the mask sets for the ASIC patterns. On the other hand, the marginal cost of producing an ASIC is usually less than that of producing a PLD because there is no wasted part of an ASIC. An ASIC is optimized for a particular function, whereas usually not all of the gates of a PLD are used once a PLD is programmed. Hence, the general belief is that PLDs are cheaper for low-volume applications and ASICs are cheaper for high-volume applications.

Types of Programmable Logic

- **Simple Programmable Logic Device (SPLD):** An SPLD is a small chip, with a series of gates and macrocells that are connected to do simple functions.
- **Complex Programmable Logic Device (CPLD):** A CPLD, which is larger than an SPLD, contains a number of pieces of circuits, each of which is like an SPLD that are connected together.
- **Field Programmable Gate Array (FPGA):** An FPGA is generally larger than a CPLD. An FPGA has a different architecture (design) than a CPLD, which enables it to do more complicated functions. FPGAs often contain memory in which data can be stored. Some FPGAs also have specialized sub-circuits (IP blocks) that are optimized for specific functions and can also be reconfigured an infinite number of times. Because of design differences from a CPLD, the complexity of an FPGA is typically measured by the number of system gates on the chip and not by the number of macrocells.

Programmable Logic Tools

To program FPGAs and CPLDs, the following tools are required:

- Programmable Read only Memory (PROM) chips are needed together with the PLDs because the PROMs contain the PLD programming. PROM memories are nonvolatile, which means that when the power is switched off, they retain the program for the PLD. In contrast, FPGAs have volatile memory on-board the chip. The PROM is needed to store all the programming information that is needed to program the PLD, as they are programmed using software-controlled switches.
- Programming software is needed to program the PLDs. Xilinx integrated software tools include the Foundation™ Series, tailored for designers who are not familiar with designing systems using FPGAs. The Alliance Series is tailored for designers who require high flexibility and integration into incumbent electronic design automation (EDA) environment, such as Cadence, Synopsis, or Mentor design software.
- IP cores: IP cores serve as plug-in modules to help customers shorten their development time and minimize design risks. IP cores implement predefined logic functions such as digital signal processing (DSP), bus interfaces, peripheral interfaces, etc.
- IRL: Reconfiguring FPGAs using Xilinx Online technology to provide time-in-market.

Looking beyond a standard PLD, Xilinx has announced a system-on-chip (SOC) initiative known as the Platform FPGA. This will mix specialized sub-circuits (hard IP blocks and soft configurable IP) with generic gate arrays or macrocells, hence making circuits that perform specific communications functions. Programmable connections between the sub-circuits and the more traditional PLD portion of the chip allows system designers to design a wide range of more powerful chips.

CPLD

What is a CPLD?

CPLDs provide designers with the capability to implement complex designs in a single chip. This replaces tremendous amounts of discrete logic devices. CPLDs may be thought of as multiple interconnected SPLDs.

An SPLD is a group of gates with interconnects that can be programmed to form desired logic functions. Invented in the early 1970s, SPLDs perform basic logic functions with limited internal resources. The basic building block of an SPLD is either a Programmable Array Logic (PAL) or

a Programmable Logic Array (PLA). This logic feeds an output cell that may be either combinatorial or registered in nature.

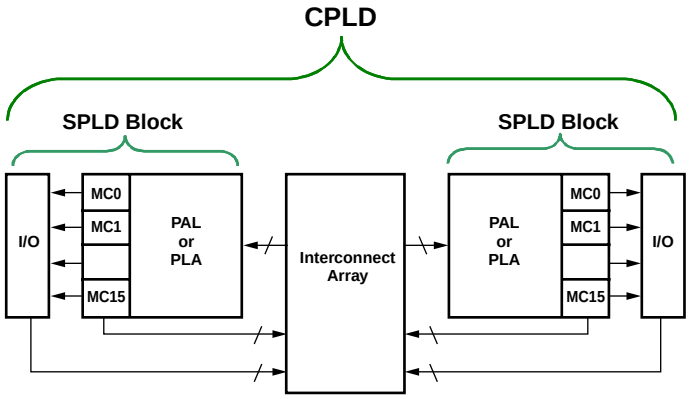

Figure 1: **Generic PLD Architecture**

CPLDs are composed of multiple SPLD blocks. The SPLD block, called a logic block, is comprised of a PAL or PLA, a macrocell, and an I/O structure. Several SPLD blocks are joined together using an interconnect array to form a CPLD. Figure 1 shows the generic CPLD architecture with multiple interconnected SPLDs. The CPLD was created in response to designers' demands for increased flexibility and feature sets.

The CPLD has many benefits, providing:

- Ease-of-design
- Low development costs
- Faster time-to-market
- Increased product revenue
- Longer time-in-market through field upgradeability
- Decreased component inventory
- Reduced printed circuit board (PCB) area
- Lower cost than discrete parts

CPLDs offer a simple way to implement a design. Once a design has been described, a designer can use CPLD development tools to optimize, fit, and simulate the design. Engineers who are spending a lot of time fixing old designs could be working on introducing new products and features—ahead of the competition. Xilinx CPLDs are divided into two families:

- The CoolRunner CPLD family that focuses on low-power, high-density CPLDs
- The XC9500 family that focuses on low-cost, high-speed CPLDs

CoolRunner CPLD Family

CoolRunner CPLDs are the first to combine very low power with high speed, high density, and high I/O counts in a single device. Xilinx CoolRunner CPLDs feature Fast Zero Power (FZP™) technology, allowing them to draw virtually no power in standby mode. CoolRunner CPLDs are ideal for battery operated portable electronic equipment such as laptop PCs, telephone handsets, personal digital assistants, and electronic games. These CPLDs also use far less dynamic power during actual operation compared to conventional CPLDs, an important feature for high-performance, heat sensitive equipment such as telecom switches, video conferencing systems, simulators, high end testers, and emulators. The entire series is available in 3.3V and 5V versions with density ranges beginning at 32 macrocells.

Traditionally, CPLDs are designed by building up a word line using "wired NOR" inputs to a node. As more of these inputs are attached to the node, the capacitance and the time constant increase. In order to speed up the propagation, this node is followed by a sense amplifier, which

examines the node for approximately a 100 mV change to indicate a logic level transition. This sense amplifier is effectively a linear element, so it is drawing a substantial amount of current even when not transitioning. A typical sense amplifier has a current consumption of approximately 250 mA per sense amplifier. This consumption increases with increased transition frequency. Figure 2 shows the sense amplifiers and Fast Zero Power for CoolRunner CPLDs.

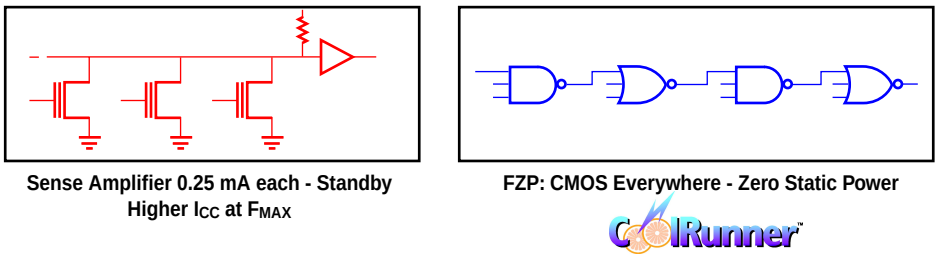

Figure 2: **Sense Amplifier and Fast Zero Power for CoolRunner CPLDs**

The CoolRunner CPLD family was designed without the sense amplifiers. The FZP technology is based on a CMOS chain of gates as the base building block for CPLD logic. The primary benefit of a technique that does not use sense amplifiers is that it results in a much lower power consumption. High speed and low power was achieved simultaneously without tradeoff for the first time in the history of CPLDs. This technology also allows for large amounts of logic resources to be placed in very small packages.

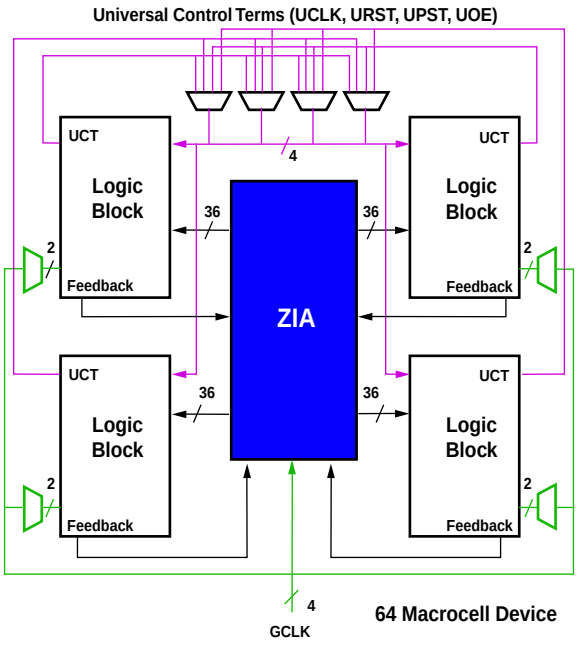

Figure 3: **XPLA3 Architecture**

At the highest level, XPLA3™ CPLDs resemble other CPLDs. Logic blocks comprised of 16 macrocells surround an interconnect array. The control and clocking of the XPLA3 device is illustrated in Figure 3. There is a pool of multiplexors distributing signals throughout the device that are used as universal control terms. A single product term is generated for this pool from each logic block and then selected by the multiplexors for a universal reset, preset, clock, and output enable.

Each logic block also provides additional internal local control terms for these operations. The local control terms are not shared among the other logic blocks. There are four global clocks

available in each device. A logic block may use any two clocks. Additional product term clocks exist for each macrocell.

Some of the essential characteristics and benefits of the CoolRunner family are:

- Fast Zero Power. No member of the family draws more than 11 mA of power during quiescent operation. The chip uses a true CMOS design so the low power is in the design.
- High density. The low power design is very compact, making these the highest density CPLDs available
- Low cost
- Low operating power
  - Longer battery live or smaller battery packs
  - Lower operating temperatures
    - Better reliability
    - Reduction or elimination of fans in the final product
    - Smaller power supply
- Smaller device packaging for less board area
  - Less expense
- Products can be made smaller making it an ideal fit for small devices such as PDAs, portable PCs, and cell phones
- Other features:
  - Early pin locking
  - Deterministic timing
  - Flexible architecture which facilitates late design changes
  - Widest product term available

XC9500 CPLD Family

XC9500™ CPLDs from Xilinx range in density from 36 to 288 macrocells and are available in 3.3V and 5V versions. XC9500 devices support in-system programming, allowing manufacturers to perform unlimited design iterations during the prototyping phase, extensive system in-board debugging, program and test during manufacturing, and field upgrades. Based on advanced flash memory technology, the XC9500 family provides fast, guaranteed timing, superior pin locking, a full JTAG (full form) compliant interface, and 10,000 programming cycles.

The advantages of the 9500XL family are speed, programming reliability, and low cost. These qualities make the 9500XL family the best at accommodating design changes while improving speed. Many industry leading architecture features are incorporated to create such flexibility. Especially important are the number of function block inputs. The 9500 has 36 inputs and the 9500XL has 54. More inputs provide better overall utilization of the device and better pin locking.

The XC9500XL family has the most complete, industry-standard JTAG boundary-scan capabilities currently available. Along with manufacturing test benefits, JTAG boundary scan enhances development and debugging, especially in complex, tightly packed systems.

The JTAG-based in-system programming (ISP) protocol allows compliance with emerging standards, such as the IEEE 1149.1 subcommittee standards for ISP.

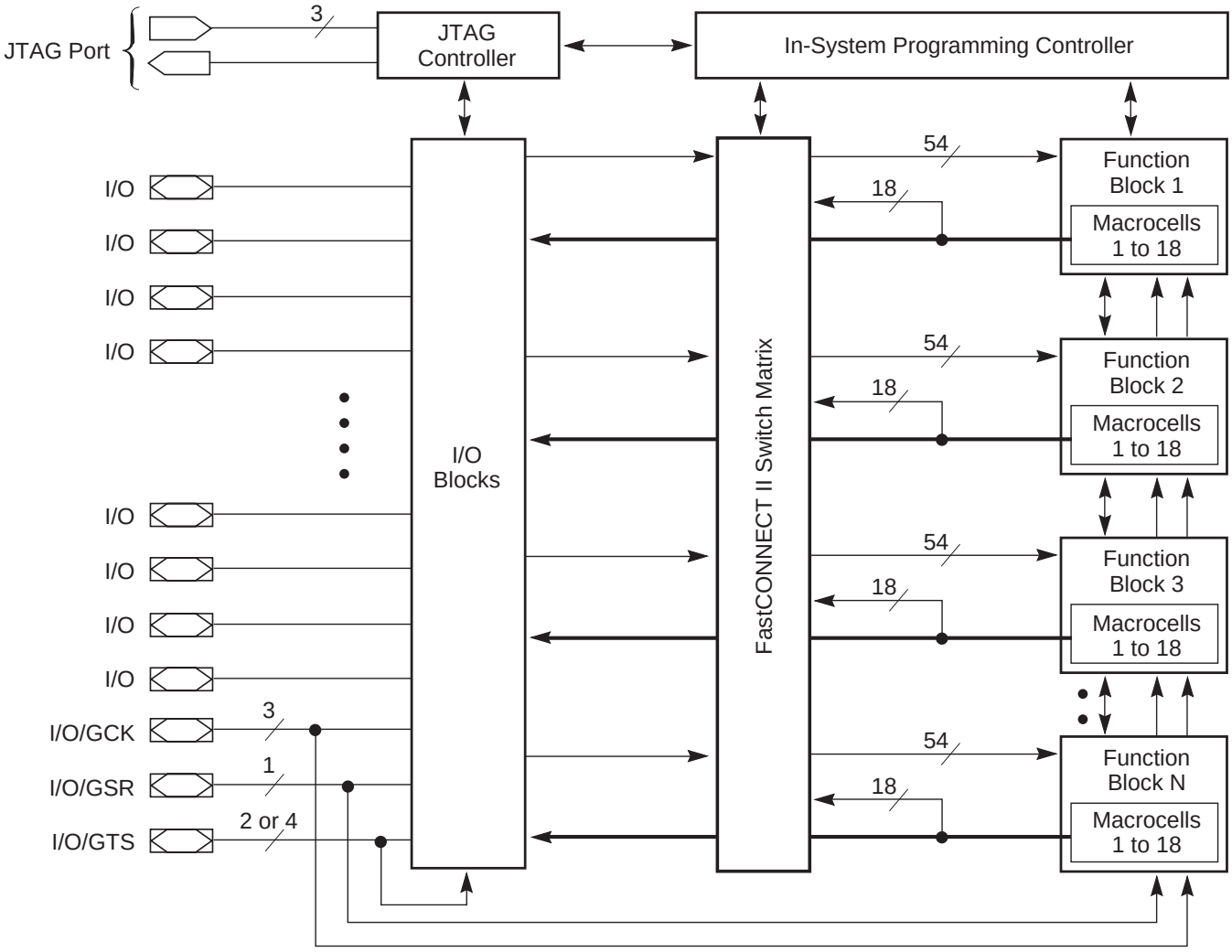

Figure 4: **XC9500XL Architecture**

As shown in Figure 4, some of the key features of the XC9500XL architecture are:

- Each macrocell independently selects clock source and phase inversion
- Clock enable at each macrocell
- Hysteresis on all inputs
- Pull-up/bus-hold option on pins at power on
- Extra-wide function block inputs
- Uniform architecture
- Identical function blocks
- Identical macrocells
- Identical I/O pins
- Abundant global/product term resources
- Optimized synthesis results
- Superior pin-locking characteristics

FPGA

What is an FPGA?

Field programmable gate arrays are field programmable devices that have logic structures which can be configured by the end user. FPGAs provide affordable solutions as customized very large system integrated (VLSI) chips, with the ability to implement logic circuits and provide instant manufacturing turnaround with very low-cost prototypes. FPGAs can be programmed in minutes to offer the same functionality and performance as ASICs/ASSPs, thus providing a significant time-to-market advantage.

The basic FPGA architecture, shown in Figure 5, is built on logic blocks and the interconnection between logic blocks and input/output blocks (IOBs).

Logic blocks have a look-up table (LUT) where the sequential circuit is implemented. The interconnection or routing structure consists of wire segments and programmable switches that connect the different logic blocks.

The IOBs provide an interface between the package pins and the internal user logic. While FPGAs today primarily consist of LUTs, interconnection, and IOBs, with the growing momentum of the system-on-chip (SOC) concept, Xilinx is leading the industry in introducing features such as processors, memory and clock management functions, and multiple I/O types.

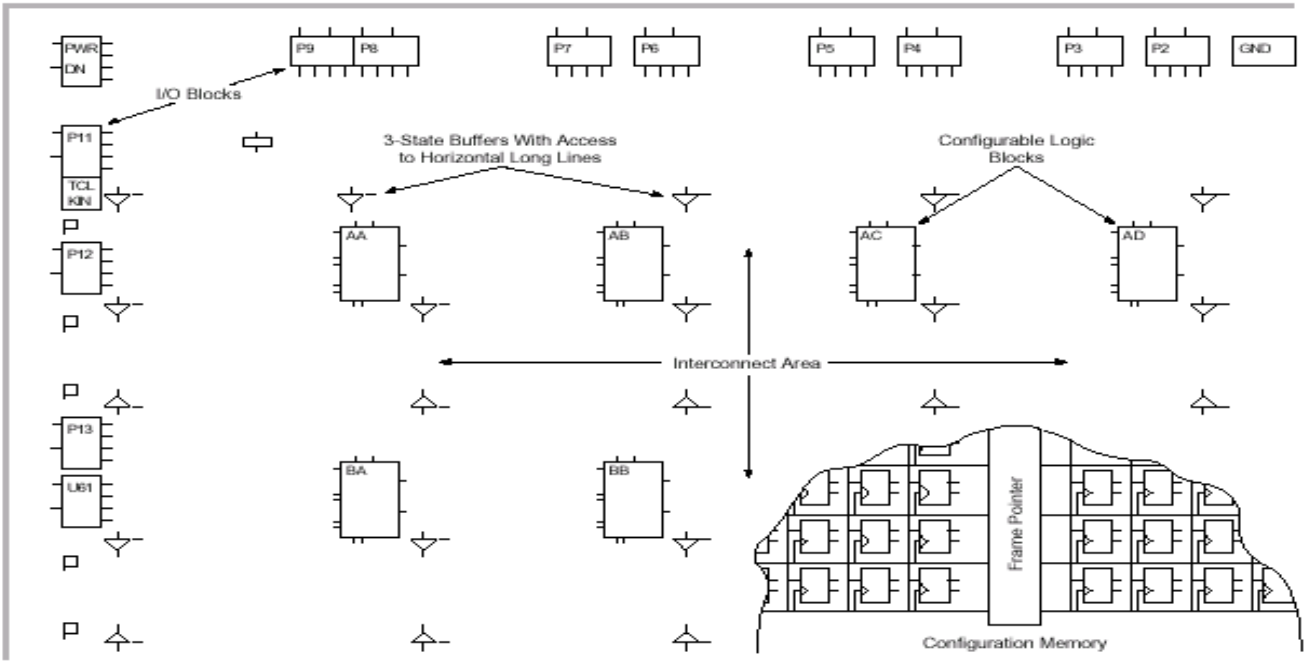

Figure 5: **Generic FPGA Architecture**

Xilinx Virtex™ series FPGAs expand the traditional capabilities of FPGAs to include a powerful set of features that address board level problems for high-performance system designs. The second generation of these devices, the Virtex-E series, is also the industry's first family of FPGAs to offer three million system gates. The Virtex series has numerous built-in features to solve designers' challenges throughout the system. This family provides a broad capability for chip-to-chip communications through programmable support for the latest I/O standards, digital delay-locked loops (DLLs) for clock signal synchronization on the FPGA and on the board, and a memory hierarchy to manage fast access to RAM on and off chip. The recently announced Virtex-II FPGAs provide densities up to ten million gates.

Spartan-II FPGAs

The Spartan FPGA series, introduced about three years ago, are targeted as gate array replacements for low-cost, high-volume designs that require on-chip RAM and can benefit from

pre-defined software cores. Spartan devices are optimized for low-cost and are available in 2.5V, 3.3V, and 5V versions. These families are based on the following philosophies:

- To use common FPGA architectures from the rest of the Xilinx FPGAs. This leverages all of the work in synthesis, software, and cores designed for that base architecture.
- To use the most advanced process technology available in order to get the smallest possible die size and lowest cost. (This is consistent with operating the transistors at a slightly larger geometry and higher voltages in order to maintain voltage compatibility with existing systems.)
- To focus on total cost management throughout the entire manufacturing flow. Most of the cost savings come from areas such as wafer sort, test, assembly, and factory logistics and overhead. At the device sizes offered in the Spartan series, the die cost is less than half of the cost equation.

The first generations of Spartan FPGAs were the Spartan and Spartan-XL families. The Spartan-II FPGA family, introduced in January 2000, is based on the very popular Virtex family. Spartan-II extends the legacy of the Spartan series, with more gates, better performance, and enhanced features. The Spartan-II family offers features such as digital delay-locked loops, programmable I/O, and on-chip block memory with densities up to 200,000 system gates. These features and densities, coupled with enhancements to software and an increased number of available IP cores, provide customers with a reduced time-to-market and increased time-in-market for the dynamic markets FPGAs serve at a much lower cost.

Spartan-II Architecture and Feature Overview

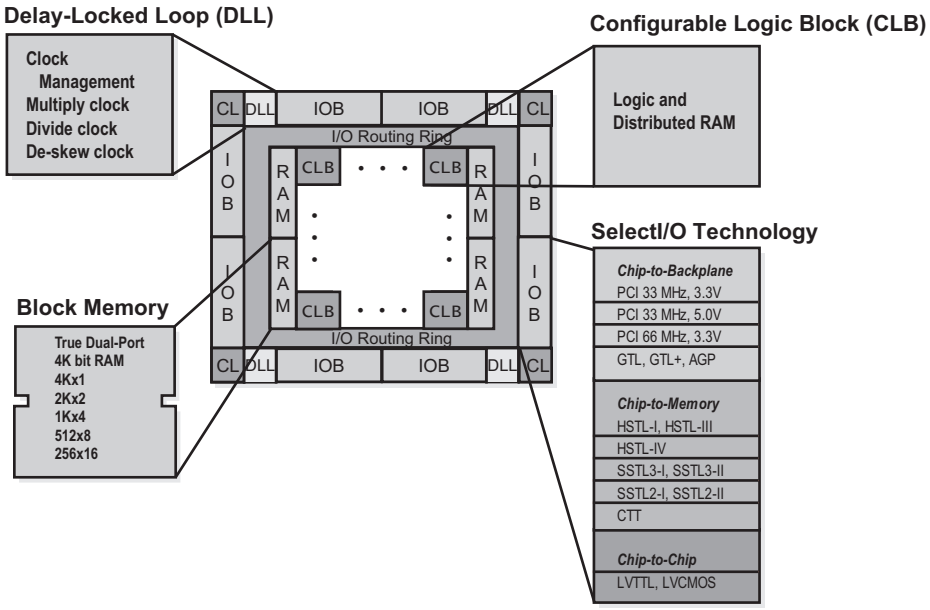

Figure 6: **Architecture and Feature Overview of the Spartan-II Family**

Figure 6 details the architecture and features of the Spartan-II family.

The configurable logic block (CLB) contains logic and distributed random access memory (RAM) that allows the performing of basic logic functions. The four DLL circuits are used for clock management and can perform clock de-skew, clock multiplication and clock division. Clock de-skew can be done on an external (board level) or internal (chip level) basis.

The block memory blocks are 4K bits each and can be configured from one to 16 bits wide. Each of the two ports can be independently configured for width. The SelectI/O feature allows many different and up to 16 I/O standards to be implemented in the areas of chip-to-chip, chip-to-memory, and chip-to-backplane interfaces.

I/O Standards

Spartan-II FPGAs support SelectI/O technology, which provides a universal I/O translation capability across many voltage levels and signaling standards. This capability is unique in the FPGA world and facilitates easy communication among chip-chip, chip-to-memory, and chip-to-backplane applications.

Figure 7 summarizes the types of I/O standards and typical applications for the three major interface groups.

- **Chip-to-chip** interfaces (LVTTL, LVCMOS) are usually used for glue logic, legacy interfaces and interfaces to other ASICs and ASSPs.
- **Chip-to-backplane** standards (PCI 32, PCI 64, GTL, GTL+) are used in processor-based systems such as those based on the Pentium CPU from Intel.
- **Chip-to-memory** standards (HSTL, SSTL) have the most variants, with different types of interfaces for static random access memory (SRAM), dynamic random access memory (DRAM), and flash memory. Since most digital consumer devices today use memory for signal processing or video/audio storage, these standards will be widely used in high-volume applications.

Type	Chip-to-Chip	Chip-to-Backplane	Chip-to-Memory	
Key Standards	LVTTL, LVCMOS	GTL, GTL+, AGP	HSTL I, III, IV	SSTL2, SSTL3
Key Highlights	Higher voltage swing	Low voltage swing	Low voltage swing, low power, low noise, 200-400 MHz	Low voltage swing, low power, low noise, SSTL3 83-166 MHz, SSTL2 166-333 MHz
Primary Usage	Legacy interface	Pentium CPU, backplanes	High-speed SRAM, MIPS/UltraSparc-II	Synchronous DRAM interface (SDR & DDR)
Applications	Glue logic, ASIC chip-to-chip	Line cards, networking, Pentium embedded applications	Line cards, graphics cards, digital cameras, modems	3-D graphics cards, plasma LCD displays, DTV interfaces, set-top boxes
Vendors	Most vendors	Intel, TI	Micron, IDT, Cypress, MIPS, IBM, etc.	Micron, Samsung, Toshiba, Hyundai, NEC, Siemens, etc.

Figure 7: **Spartan-II SelectI/O Technology**

Xilinx I/O solutions give you the flexibility to easily design the I/O in many different situations. Since these solutions are standardized, the customer's time-to-market is reduced. This also saves board area by eliminating the need for level translators.

Delay-Locked Loop Technology

Spartan-II FPGAs include powerful chip and board level clock management capabilities with DLL circuits. DLL is the digital implementation of an analog phase-locked loops (PLLs). The Spartan-II family includes four DLLs in each device, with each DLL having capabilities to remove on-chip and board level clock delays. This allows you to get clock-to-out times of less than 3.5 ns on even the largest Spartan-II device.

Using these clock management functions can save system costs by allowing slower speed clocks on the board (which are then multiplied by the DLL internally) or through the use of slower access time memories (since the internal clock delays are reduced and chip performance improved). This lowers the memory and board costs.

Electro-Magnetic Interference (EMI) Friendly

Xilinx parts are designed to have very low emissions and, hence, reduce the risk of EMI in any design.

On-Chip Memory

Spartan-II FPGAs have the following two types of RAM within the devices:

- Distributed SelectRAM™, that are implemented in look-up tables, are suitable for shallow

memory structures and small FIFOs.

- Block SelectRAM, that are dedicated RAM blocks, have depths and widths that are parameterizable. The block SelectRAM is excellent for applications that require larger blocks of memory such as large FIFOs and buffers, video line buffers, or packet buffers in small office routing equipment.

In addition, Spartan-II SelectI/O™ standards allow fast access to external memory interfaces for applications that require blocks of memory in the MB and more range. DLLs lower the need for off-chip clocking resources, while on-board memory reduces the need for external buffer memory. A combination of these features helps lower the overall system-level cost. The Spartan-II delivers all the essential requirements for ASIC replacement:

- Low cost
- Densities up to 200,000 gates
- Internal speeds of 200 MHz
- Flexible I/O interfaces
- On-chip distributed and block RAM
- Clock management
- Complete development system support
- Less EMI issues

IP Solutions: System-Level Designs for FPGAs

Today, a large number of predefined cores are available to implement system-level functions directly in Xilinx PLDs. These cores, available from Xilinx and third-party partners, allow designers to cut design time and significantly reduce risk while having access to the best performing and lowest cost components available. Full information about Xilinx cores is available online from the IP center area of the Xilinx website. To get to the IP center, log on to:

www.xilinx.com/ipcenter

LogiCORE™ products are sold and supported directly by Xilinx and include IP cores such as system interfaces such as PCI, digital signal processing (DSP) functions, and a number of other modules such as adders, multipliers, and look-up tables. These IP cores are optimized for Xilinx FPGAs and CPLDs to provide the fastest speeds while utilizing minimum board area.

AllianceCORE™ modules are sold and supported by a network of third-party developers and are optimized for Xilinx devices. This program has allowed Xilinx to expand the availability of high-quality cores for PLDs through a cooperative effort between Xilinx and independent third-party cores developers. Current AllianceCORE products range from processors and standard peripheral controllers to ATM functions. Xilinx takes an active role with its partners in the process of cataloging AllianceCORE products. This is unique to the AllianceCORE program. Because the process is so involved, we work closely with our partners to select the right cores first which helps raise the quality and usability of the cores that are offered. A core must meet a minimum set of criteria before it can receive the AllianceCORE label.

Smart-IP™ technology is a combination of several features designed to deliver the highest performance, predictability, and flexibility when implementing IP with Xilinx FPGAs. Smart-IP technology ensures constant core performance regardless of its position in the FPGA device; maintained performance when multiple cores are integrated in the same FPGA device; and no performance degradation when migrating to larger devices. The IP is built to utilize the unique features of the Spartan-II architecture such as dedicated multiplier or multiplexor logic. The use of Smart-IP technology means that the performance of the core is independent of core placement, number of cores used, surrounding user logic, device size, and EDA tools.

The CORE Generator™ tool from Xilinx delivers highly optimized cores that are compatible with standard design methodologies for Xilinx FPGAs. This easy-to-use tool generates flexible, high-performance cores with a high degree of predictability and allows customers to download future core offerings from the Xilinx website. Both Xilinx and independent IP developers can

design cores for the CORE Generator tool, which also serves as a cataloging and delivery system for related collateral for all designers using Xilinx.

Internet-Enabled Software Solutions

Leading-edge silicon products, state-of-the art software solutions, and world-class technical support make up the total solution delivered by Xilinx. The software component of this solution is critical to the success of every design project. Xilinx software solutions provide powerful tools which make designing with programmable logic simple. Push button design flows, integrated online help, multimedia tutorials, plus high performance automatic and auto-interactive tools help designers achieve optimum results. And the industry's broadest array of programmable logic technology and EDA integration options deliver unparalleled design flexibility.

At Xilinx, software tools are a key part of the company's programmable logic solutions. Since its inception, Xilinx has shipped more than 60,000 development systems to customers worldwide. Today, Xilinx offers two software products for design and implementation that are Internet-enabled to allow designers instant and direct access from the tools to the technical support area of the Xilinx website.

Through its Alliance Series™ software, Xilinx has chosen an open system approach that allows its customers to pick the highest quality and widest variety of design and programming tools available on the market today. To accomplish this, Xilinx has established engineering and marketing relationships with the leading third-party suppliers of electronic design automation (EDA) software. Those include Aldec, Cadence, Data I/O, Exemplar, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest, and Viewlogic. This open systems strategy extends to front-end design creation, synthesis, and verification. The result has been the creation of complementary technology and tightly integrated third-party links with the Xilinx Alliance Series backend place-and-route software for FPGAs and CPLDs.

Foundation Series™ is a family of a fully integrated, ready-to-use Windows PC tools that support a broad range of FPGA and CPLD design requirements. Available at low cost and targeted at entry-level as well as high-end users, the Foundation Series products leverage industry standard hardware description languages (HDLs), including Verilog/VHDL. The Windows-based Foundation Series software provides access to synthesis, schematic entry, gate level simulation, and implementation tools. Since Foundation Series tools are integrated into a common design management environment, users have access to all technology from design entry and implementation to verification in a single software package.

WebFITTER™ is a unique Internet-based software productivity tool that permits customers anywhere in the world to do online fitting of CPLD designs from their PC or workstation. WebFITTER kicked off the Xilinx "Silicon Xpresso Initiative" that calls for stepped use of the Internet to help increase designer productivity.

Designers access WebFITTER from the Xilinx website and work from a graphical user interface integrated with the Netscape browser. WebFITTER produces complete online reports for design evaluation, and it eliminates the need for designers to load software or manage updates and licenses because the latest Xilinx tools always reside on the Xilinx website. WebFITTER accepts design files for Xilinx XC9500 and CoolRunner series complex programmable logic devices (CPLDs) and supports VHDL, Verilog, ABEL, XNF, or EDIF input formats. After completing a front-end design, users simply enter their e-mail address, attach their design file and send it to the Xilinx server for compilation. Shortly after, a return e-mail provides a complete fitter report and bitstream to implement the design in the PLD. To get to the WebFITTER tool, log on to:

www.xilinx.com/sxpresso/webfitter.htm

The Xilinx WebPACK™ contains FREE downloadable software solutions for Xilinx XC9500 and CoolRunner Series CPLDs. Each solution provides a simple and intuitive design environment for any Xilinx CPLD family. The WebPACK is a collection of three design suites: design entry, device fitting, and programming. These tools can be downloaded and used individually or, when installed together become an integrated design environment for Xilinx CPLDs. To download WebPACK software solutions, log on to:

www.xilinx.com/sxpresso/webpack.htm

Xilinx Online and Internet Reconfigurable Logic (IRL)

Xilinx is pioneering a paradigm shift with the ability to remotely update FPGAs and hence hardware for systems already deployed in the field. The Xilinx Online program is designed to enable, identify, and promote network upgradeable systems, hence future proofing a system. These are systems that can be upgraded, modified, or fixed after they have been deployed in the field. While many customers have been building upgradeable devices based on Xilinx technology for years, the explosion of the networked connected devices has dramatically increased the demand for these user configurable and adaptable applications.

As an example, an engineer can reprogram and remotely upgrade a cellular base station with the latest specification and standard in a matter of minutes over the Internet using a Xilinx FPGA in the system. Having the ability to remotely update hardware with new features or the latest bug fix can accelerate the time-to-market of an application, extend the useful life of existing systems, and significantly cut production, maintenance, and support costs. Many of today's systems have available some form of communications and/or microprocessor interface built in, making the addition of remote field update capability a simple matter. If designers consider remote updates during the initial specification/design process, their systems can easily reap all of these benefits.

Xilinx provides IRL technology to make it easier to develop these systems based upon the most advanced programmable logic available.

Technical Support

Xilinx provides 24-hour access to a set of sophisticated tools for resolving technical issues via the Web. The Xilinx search utility scans thousands of Answers records to return solutions for the given issue. Several problem-solver tools are also available for assistance in specific areas, like Configuration or Install. A complete suite of one-hour modules is also available at the desktop via live or recorded e-Learning. Lastly, users with a valid service contract can access Xilinx engineers over the Web by opening a case against a specific issue. For technical support on the Web, log on to:

support.xilinx.com

Xilinx is committed to helping users succeed with programmable logic designs and provides a complete and uniquely accessible array of services and training for customers with service contracts. Xilinx experts provide responsive resolutions to problems and creative, timely solutions to design challenges. They also offer design evaluation of new projects and close consultation through the design process. Full training in design completion and methodology review is also available, along with special application consultation.

Xilinx at Work (XaW)

XaW is a vertical marketing effort providing customers with comprehensive solutions, tutorials, and reference designs for networking, telecom, wireless, embedded, and consumer high-volume markets. XaW™ highlights complete solutions of devices, software, and IP cores/services along with an illustration of how Xilinx adds value in designs for particular application segments. Specifically, the XaW team produces:

- Technical and market analysis
- Collateral: White papers, application notes, tutorials
- Glossaries
- Articles for Xcell™ Quarterly Journal and other trade publications
- Reference designs
- Web solutions
- Presentations and representations at exhibitions and conferences

The XaW team has put together solutions for various applications, such as:

- Set-top boxes, MP3/Internet audio players, smart card readers, printers

- Digital modems: xDSL, satellite, ISDN
- Embedded memory and memory controllers: QDR SRAM, SDRAM, SRAM
- IMA (Inverse Multiplexing for ATM)
- FIR filters, 64- and 32-bit PCI solutions, encryption: DES and triple DES, video and imaging: DCT/IDCT, HDLC, Reed-Solomon, 8-bit microcontrollers

More information on Xilinx at Work and the applications is available at:

www.xilinx.com/products/xaw/

Advantages of Spartan-II FPGAs for Home Networking

Spartan-II FPGAs can provide functionality and performance comparable to competing ASSPs, with the flexibility required in today's consumer applications. Spartan-II FPGAs are the perfect programmable system integration and interface vehicles, providing a high-bandwidth communication interface to external devices such as ASSPs, CPUs, memory, and backplanes. This eliminates the need for custom logic, expensive clock management schemes, and various translator components including direct interface to backplanes such as GTL I/O capability. The Spartan-II family integrates simple ASSP functions such as PLLs, FIFOs, level translators, and others which can save the user considerable cost.

Spartan-II FPGAs, with the low-cost, high-density, and increased feature content are ideal for evolving markets.

The dynamic home networking market is demanding that products be brought to market at competitive prices. The broadband access devices, residential gateways, home networking products, and information appliances are products that have in some form existed before. Today they require one or more home networking interfaces while specifications and standards continue to develop products need to be brought to market. While developing ASSPs takes 12-18 months, a Spartan-II FPGA programmed with the appropriate IP can perform ASSP functionality. A unique role for the Spartan-II FPGA is providing an interface to the different ASSPs. This technology bridging function is crucial in the home networking market where multiple technologies and ASSPs with different interfaces.

Spartan-II FPGAs facilitate and enable home networking solutions because FPGAs are reprogrammable and hence, offer several advantages over ASICs and ASSPs:

- No manufacturing leadtime for the silicon helps reduce time-to-market
- Reprogrammability means any bug fixes and standards updates can be easily implemented, ensuring longer time-in-market for customers

Xilinx FPGAs are the superior FPGA solution since they have industry leading speed, density, power, and cost features. Xilinx FPGAs and core solutions allow you to turn the chaos in the home networking market into an opportunity to:

- Get to market faster (no hardware lead time)
- Make changes to product features (reprogrammability)
- Update a product to a new standard faster (reprogrammability)
- Increase customer satisfaction and thereby increase market share by field upgrading to fix bugs, add new features, or fit a changed standard
- Use core solutions to speed the design time of new products
- Use the inherent flexibility that programmable logic offers for:
  - Product customization to meet customer needs
  - Adaptation to specification updates
  - Feature upgrades
  - Low risk evaluation of new markets
- The ability to upgrade products remotely once they have already launched into the field.

As specifications change, traditional ASSP vendors do not have the ability to provide an ASSP to address the dynamic nature of an application. Xilinx FPGAs, with the ability to be

reprogrammed, are ideal for this purpose. Designing an FPGA within your system can save costs and decrease board size significantly.

An example describing the value of programmability at low cost is in using a Xilinx FPGA instead of a PCI ASSP. A standard design might use many chips such as external PLD, external DLLs, memory, memory controllers, I/O translators, and a PCI master and slave interface PCI ASSP. A design using a Spartan-II FPGA with a PCI LogiCORE IP can replace many chips with a single Spartan-II, hence providing lower costs and decreased board size.

IP for Spartan-II FPGAs

The Spartan-II family has had very robust core support since the time of its introduction. Xilinx has a range of IP cores such as memory controllers, system interfaces, DSP, communications, networking, and microprocessors.

The extensive Spartan-II IP library includes the following cores:

- **BaseBlox:** UARTs, multipliers, DMA
- **Memory/memory controllers:** SRAM controllers, SDRAM controllers
- **Networking and communications:** Cell assembler, cell delineation, CRC, T1 Framer, HDLC controllers, 10/100 Fast Ethernet, UTOPIA, ATM/IP over SONET, ADPCM, IMA, SONET, OC-48, OC-192, VoIP, Reed-Solomon FEC, Viterbi FEC, xDSL modems, cable modems, satellite modems, UMTS, W-CDMA
- **Microcontrollers, microprocessors:** 8051, 8-bit, 32-bit RISC processors
- **DSP:** FIR filters, comb filters, FFT, color space converter, DCT/IDCT video and image processing, DES, Triple DES, MP3, QAM, QPSK, JPEG, speech recognition, programmable DSP engines
- **System I/O, standard bus interfaces:** Two-wire serial interface, CAN (Car Area Network), ISA, I2C, PCI (32- and 64-bit, 33 and 66 MHz), Compact PCI Hot-Swap, PC-104, VME, AGP, USB/USB2.0, IEEE 1394/FireWire, PCI-X 133 MHz, and other emerging high-speed standard interfaces

Xilinx is currently developing several IP cores to address the home networking and consumer markets.

Emerging Standards Program (eSP)

The digitization of consumer and communications technologies is necessitating the establishment of new standards and protocols. Examples, explaining the need for standards and protocols include:

- **Wireless communications standards:** IEEE 802.11, HomeRF, and Bluetooth
- **Serial digital communications standards:** IEEE 1394 (FireWire), USB/USB 2.0, Optic Fiber, Gigabit Ethernet, 10 Gigabit Ethernet, RapidIO, Lightening Data Transport (LDT), and Infiniband
- **Streaming communications technologies:** Internet audio playing (MP3), video content distribution, and interactive conferencing

These technologies are progressing in “Internet time,” placing extraordinary challenges and pressures on system architects and ASIC/ASSP/FPGA designers for new product development. While the need to develop products and introduce them to market are important, understanding the technology and standards to make the right decisions are paramount. The value proposition of programmable logic solutions is in helping designers in addressing the challenges, such as:

- **Dealing with multiple standards:** Typically, more than one alternative (standard) is available to address any given challenge. This introduces tremendous risk in selecting a solution because many contenders will not succeed in the long term. *Programmable logic solutions, while not exempt from this risk, require less time investment and can adapt to newer architectures and standards.*
- **The extensive scope and complexity of emerging technologies:** The specifications for

emerging technologies are correspondingly large and subject to ambiguity and error. They are new and unproven. This virtually mandates a development cycle where the implementation is cycled through numerous prototype, test, and debug iterations before it becomes stable. *Programmable logic is virtually the only way to produce such designs efficiently.*

- **Emerging standards need to be updated on a regular basis:** As much as the designers try to maintain backward compatibility, this cannot be guaranteed. *Programmable logic solutions are virtually the only platform that can remain viable over time.*
- S**hrinking development cycles:** Manufacturers realize that to achieve maximum success they must get products to market as quickly as possible. *Programmable logic is the superior alternative for fast time-to-market.*

The Xilinx eSP initiative is a program designed and tailored to address primarily these issues. eSP focusses on digital consumer convergence markets and is targeted at system architects and ASIC/FPGA designers to:

- Help them understand these technologies
- Evangelize the benefits of programmable solutions
- Provide support resources for Xilinx-based solution options

eSP assists customers shorten the time-to-market for emerging standards and protocols. The traditional time-to-product advantage of FPGAs is well known. eSP further accelerates the time-to-learn and time-to-design period in product development (Figure 8). eSP provides customers and system developers with standards tutorials, white papers, application notes, system solutions, IP, and more in these dynamic markets. This helps in understanding the technology and specifications and making the right decisions in designing products. The first eSP segments will be home networking and Bluetooth.

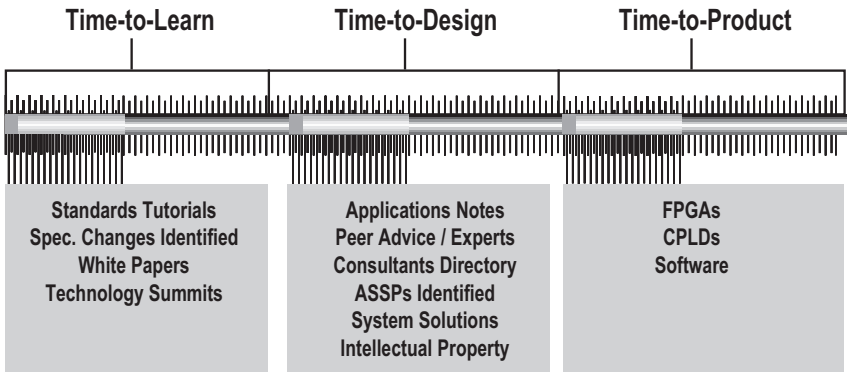

Figure 8: **eSP—Accelerating Time-to-Learn and Time-to-Design, and Hence Helping Reduce the Customer's Time-to-Product**

eSP is the industry's first Web portal dedicated solely to addressing the challenges of developing products based upon emerging standards and protocols (Figure 9). eSP simplifies the task of designing your next product by delivering a complete set of solutions aimed at accelerating the time-to-market for your next product.

eSP delivers a complete suite of solutions that accelerate the development time of products based on emerging standards and protocols.

Figure 9: **eSP Program Details**

Standards Tutorials

A major focus of the eSP initiative is to help designers get an overview of the various specifications and to understand the complexities associated with them. The tutorials are carefully crafted to contain enough detail and at the same time to also not overwhelm the designer. The material also caters to a wide audience ranging from the curious to the serious system architect. As an example, every major aspect to the home networking market segment is covered in 2,600 carefully documented pages of tutorials. The topics covered includes market research, overview of the various technical specifications, the hurdles faced by designers, projections on the future, system block diagrams, industry links, FAQs, and a detailed glossary, all available directly through the Internet.

Keeping Current on Changes

One other key feature of the eSP initiative is that it allows you to learn about the changes to standards and protocols as they happen and, more importantly, understand the impact on your product design. Truly, a one-stop shop to get an update on all the specifications related to a specific consumer market segment.

Ask the Experts

Xilinx has put together a panel of experts to answer your most pressing questions. Each market segment explored and discussed under the eSP initiative has its very own discussion forum. Staffed by some of the industry's leading experts, chances are that we probably have the answers to the toughest design challenge questions. As an example, the home networking effort has more than ten experts on the panel with a very strong understanding of the home networking industry.

Application Notes, White Papers, and Glossary

Whether you need to learn even more about a standard or protocol, or you are simply trying to figure out what a term means, eSP can help. You are likely to find an application note or white paper on the very topic you are looking for. The eSP website contains application notes and white papers that include in-depth discussions market and technical analysis, and are

constantly updated to keep you current with the latest changes in the industry. The website also contains an extensive glossary of more than 1,000 terms to quickly understand acronyms and definitions of industry terms.

System Block Diagrams

If you are trying to figure out the best way to build your next product, simply peruse our system block diagram pages. The eSP website has a very extensive set of system block diagrams and the home networking market segment offers over 60 block diagrams that cover broadband access devices, residential gateways, home networking technologies, and information appliances.

Intellectual Property

The eSP program identifies important IP required for the system architects and ASSP/FPGA designers to succeed in a market where standards and specifications are evolving. Working through the LogiCORE and AllianceCORE programs, the eSP team will provide a broad selection of industry-standard IP cores and solutions dedicated for use in Xilinx programmable logic.

Strategic Alliances—The Ecosystem Era

System designers face many obstacles to design consumer products in an environment where standards continue to evolve. This makes the selection of critical system components extremely challenging. Xilinx has introduced a new approach to creating cutting-edge complete systems solutions that offer customers sustainable competitive advantage—the eSP ecosystem.

The eSP ecosystem consists of Xilinx and industry leaders that jointly strive to provide complete system solutions. Each member of the ecosystem brings their own unique expertise, core competency, and strength. Together, the ecosystem is committed to developing and offering unparalleled complete innovative solutions that enhance customer productivity. More importantly, the solutions developed will completely comply with the relevant emerging standards and protocols. Since, this is an integral part of eSP, the ecosystem is committed to providing a update path to future standards and protocols. An example of a typical eSP ecosystem is shown below in Figure 10.

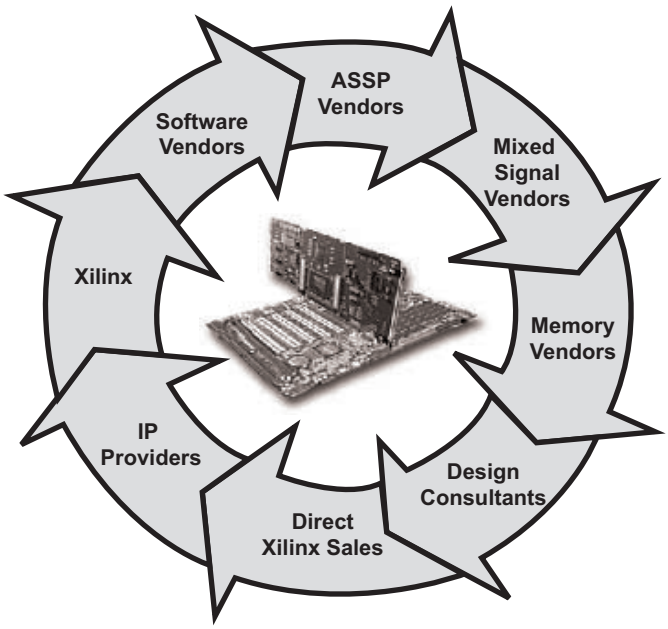

Figure 10: **The Xilinx eSP Ecosystem**

Home Networking—An Ecosystem Example

The home networking market provides a great example of how effective the eSP ecosystem can be. There are many home networking standards, which are currently evolving, for example, IEEE 1394a to IEEE 1394b, HomeRF, HomePNA, HomePNA 2.0, and HomePlug, among others.

Let's take an example of a residential gateway. To design a successful residential gateway, a manufacturer must decipher and comprehend complex standards. There are many decision points:

- What broadband access technology should the residential gateway support:
  - Cable modems
  - xDSL modems
  - Satellite modems
  - Wireless modems
- What home networking technology should the residential gateway support:
  - IEEE 1394a, IEEE 1394b
  - HomePNA
  - HomePlug, X-10, LONWorks
  - HomeRF
  - Bluetooth
  - Wireless LAN: IEEE 802.11a, IEEE 802.11b, HiperLAN2
  - USB 1.1, USB 2.0
  - Ethernet
  - Fiber Optics LAN Section (FOLS) of the Telecommunications Industry Association

To make the problem more complex, the technology required for each solution is typically available from more than one vendor. In addition, one vendor's solution is not always optimized to interface with another vendor.

Enter Xilinx and the eSP ecosystem—the solution to the problem. The ecosystem involves strategic alliances with industry leaders to jointly provide a proven residential gateway design that meets and conforms to all of the industry standards. Moreover, the very nature of programmable logic allows the eSP ecosystem to construct the residential gateway so that it can be upgraded in the field to support fast implementation of changing standards. Of course, the eSP ecosystem also works very closely to insure that everybody's solutions provide transparent interoperability.

However, the solution does not stop there. The eSP ecosystem is also committed to providing all the necessary support, whether it is hardware or software. The customer can use the proven design as is, or make any modifications for product differentiation by utilizing the "spare programmable logic gates" or by using vertical migration (a method of using higher density programmable logic devices in the same package, without changing the pinout).

The real advantage of the eSP ecosystem is that every member of the ecosystem benefits. Each ecosystem member also gains expanded market coverage, because all ecosystem members promotes proven designs through their own sales and marketing channels.

System Solutions (Reference Designs)—Tying it All Together!

As part of the eSP initiative, Xilinx has partnered with a wide range of industry experts, ASSP manufacturers, and IP providers to develop, deliver, and support hardware reference designs for specific emerging standards. These reference designs accelerate product development while addressing the flexibility and price constraints of the targeted end application.

These are not just reference designs, however. They are complete system solutions designed to conform to all of the necessary standards and protocols. The reference designs are tested to comply with industry consortia specifications as well as the relevant standards bodies. These system solutions contain everything necessary to build and develop the final product. The reference designs include:

- Bill of materials
- Gerber files
- Software
- Software drivers
- Hardware
- VHDL or Verilog code
- Programming software
- Design tools
- IP cores
- Datasheets
- Schematics
- Applications notes
- License agreements

Because the system solutions are based upon the low-cost Spartan-II FPGA family, the reference design can be easily customized for product differentiation or to add extra features.

The eSP initiative extends the traditional benefits of flexibility and time-to-market offered by FPGAs. Moreover, the initiative helps with the learning and design phases of product development. The eSP initiative provides revolutionary solutions for products dependent on emerging standards and protocols. Because eSP and Xilinx solutions take the guesswork out of understanding these standards, Xilinx customers can focus on the important matters like product development and product marketing. You will find everything you need to get ahead and stay ahead of emerging standards and protocols at your fingertips:

www.xilinx.com/esp/

While the first segment of eSP is home networking, the team is developing solutions for Bluetooth, digital cinema, automotive, infotainment and other consumer segments.

eSP: Home Networking

The home networking market, while emerging and chaotic, is fast growing. The Xilinx eSP: Home Networking program provides the user information on the multiple standards and technologies that make up home networking—broadband access, residential gateways, home networking technologies and information appliances. The components addressed as part of this program (shown in Figure 11) are:

- Broadband access:
  - Digital modems: satellite, cable, xDSL (ADSL, SDSL, HDSL), powerline, wireless
  - Analog phonelines dial-up modems
- Media or residential gateways:
  - Set-top boxes
  - SOHO routers
  - Home servers
  - PCs
  - Gaming consoles
  - Digital modems
- Home networking technologies:
  - No new wires: phonelines, powerlines
  - New wires: Optic fiber, FireWire/1394, USB/USB 2.0, Ethernet
  - Wireless: Bluetooth, HomeRF, wireless LANs (IEEE 802.11a, IEEE 802.11b, HiperLAN2)
- Information appliances:

- Digital TV (HDTV)
- Digital displays (PDPs, LCDs)
- Digital VCR
- Gaming consoles
- Set-top boxes
- Internet screen phones
- Internet audio (MP3) players
- Security systems, utility meters
- Web pads, web terminals, e-mail terminals
- PDAs
- Digital cameras, printers, scanners
- Auto PCs

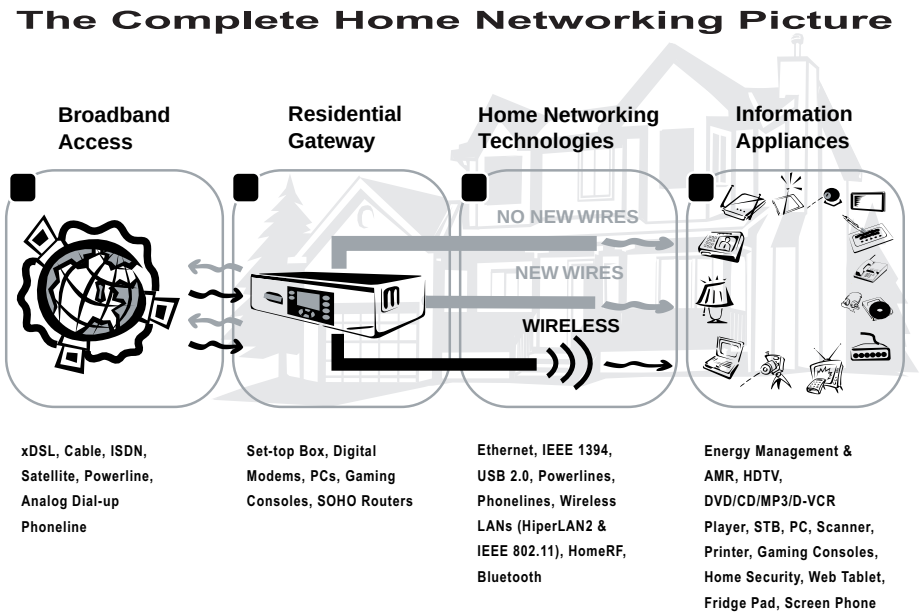

Figure 11: **Four Aspects to Home Networking**

The recently launched eSP: Home Networking initiative will help our customers reduce their time-to-market for emerging standards and protocols. This program will help accelerate the time-to-learn and time-to-design period in product development for broadband access, home networking, residential gateway, and information appliance products. This Web portal is dedicated to provide information on standards tutorials, white papers, application notes, system solutions, required IP, and other solutions for the dynamic home networking markets.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/21/01	1.0	Initial Xilinx release.