Configuration Control Pin Connections in

The following recommendations guarantee a well-defined beginning for any FPGA configuration or reconfiguration process — after the initialization and clearing of the configuration memory in all FPGAs has been completed, and the address counter in the serial PROM(s) has been reset. Previous versions of the Xilinx Data Book have shown different solutions, but the connections described below guarantee reliable operation even under adverse operating conditions such as V_{CC} glitches.

The lead device can use any configuration mode available. In master modes and Asynchronous Peripheral mode, its CCLK pin is the output that clocks all other devices.

Obviously, all CCLK and XC17000 CLK pins must be interconnected, the DATA outputs from multiple XC17000 serial PROMs must be interconnected and connected to the DIN input of the lead device. The daisy-chain must be established by connecting each DOUT output to the downstream DIN input.

The following recommendations assume that there are no XC2000 devices in the daisy chain (they lack the $\overline{\text{INIT}}$ pin) and that, if Serial mode is chosen for the lead device, the XC17000 device(s) store **only one** configuration for the whole daisy chain. The serial PROM(s) must, therefore, be reset before the daisy chain is to be (re)programmed.

There are three possible types of daisy chains using XC3000 and XC4000 devices. Here are the recommended connections for the configuration control pins.

Configuration control pins are:

- **XC3000, XC3000A, XC3100, XC3100A**
  DONE/$\overline{\text{PROGRAM}}$ (open-drain output/input)
  $\overline{\text{RESET}}$ (input)
  $\overline{\text{INIT}}$ (open-drain output)
- **XC4000, XC4000A, XC4000D, XC4000H**
  DONE (open-drain output/input)
  $\overline{\text{PROGRAM}}$ (input)
  $\overline{\text{INIT}}$ (open-drain output/input)
- **XC17000**
  RESET (input with programmable polarity)

Case 1

Daisy chain consists of nothing but XC3000-type devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all slave $\overline{\text{INIT}}$s and connect them to the lead $\overline{\text{RESET}}$ input.
- Interconnect all DONE pins.
- Interconnect all slave $\overline{\text{RESET}}$ inputs
- Instigate **Reprogram** by pulling the slave $\overline{\text{RESET}}$ net Low for at least 6µs while all DONE pins are Low. (DONE can be permanently wired Low, but that sacrifices the use of $\overline{\text{RESET}}$ as a global reset of the user logic. If DONE is not wired Low, reprogram must pull DONE Low with an open-collector or open-drain driver).

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FPGA Daisy Chains

Case 2

Lead device is XC4000-type, driving any mixture of XC3000 and XC4000 devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all $\overline{\text{INIT}}$ pins.
- Interconnect all DONE pins.
- Interconnect all XC4000 $\overline{\text{PROGRAM}}$ inputs.
- Interconnect all XC3000 $\overline{\text{RESET}}$ inputs.
- Combine these two nets into one $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ net
- Instigate **Reprogram** by pulling the combined $\overline{\text{PROGRAM}}$/$\overline{\text{RESET}}$ Low.

Case 3

Daisy chain consists of nothing but XC4000-type devices:

- Use lead device's $\overline{\text{LDC}}$ to drive XC17000 $\overline{\text{CE}}$.
- Use lead device's $\overline{\text{INIT}}$ to drive XC17000 $\overline{\text{RESET}}$.
- Interconnect all $\overline{\text{INIT}}$ pins.
- Interconnect all DONE pins (only required for UCLK-SYNC option).
- Interconnect all XC4000 $\overline{\text{PROGRAM}}$ inputs.
- Instigate **Reprogram** by pulling $\overline{\text{PROGRAM}}$ Low. ◆