# Examining XC4000E RAM Capabilities

Although it provides increased performance and several new features, each member of the new XC4000E FPGA family is pin- and bitstream-compatible with its corresponding XC4000 cousin.

While maintaining all of the XC4000's capabilities, the XC4000E adds these prominent new features:

- Distributed on-chip RAM
- Synchronous or edge-triggered RAM writing that simplifies timing and improves performance. Careful timing relationships between address, data, and write enable are no longer required.
- Dual-port RAM mode that provides simultaneous read/write capability. This mode is especially useful for building FIFOs and buffer memories. Dual-port RAM is always edge triggered.
- The ability to pre-initialize the contents of RAM on power-up. This feature simplifies an overall design in that RAM values are automatically defined. No additional logic is required to perform the initialization.

Table 1 describes the relative capabilities of the XC4000 and XC4000E families.

Using the new capabilities, memory-based designs operate at much higher speeds. For example, a First-In, First-Out Memory (FIFO) can double in speed when implemented with edge-triggered RAM compared to level-sensitive RAM. Designs can take advantage of the edge-triggered functionality to eliminate input data registers, significantly reducing the size of the circuit.

Dual-port mode allows simultaneous reading and writing, effectively quadrupling the speed of a FIFO over level-sensitive implementations (a first doubling as a result of edge-triggered write, and a second doubling due to the dual-port mode).

**Table 1.** *RAM Capabilities of XC4000 and XC4000E*

| Feature | XC4000 | XC4000E |
|---|---|---|
| On-chip RAM | ✓ | ✓ |
| Level-sensitive RAM write | ✓ | ✓ |
| Single-port capability | ✓ | ✓ |
| Dual-port capability | | ✓ |
| Edge-triggered RAM write | | ✓ |
| Initialized RAM data at power-up | | ✓ |

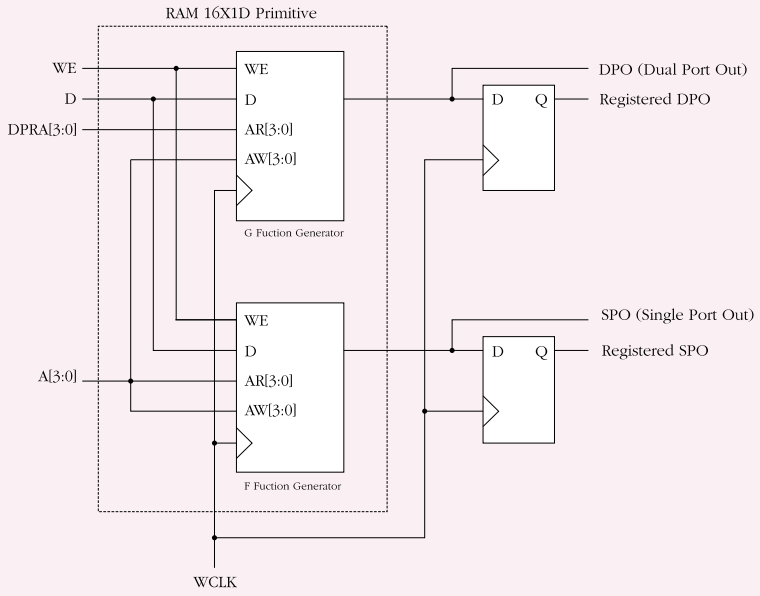


**Figure 1:** *Conceptual model of dual-port memory implemented in an XC4000E CLB.*

## XC4000E Conceptual Model

Figure 1 shows a conceptual model of the XC4000E RAM, configured as a 16x1 dual-port, edge-triggered RAM.. This diagram will be used to describe the various edge-triggered and dual-port capabilities available within each XC4000E logic block. (The diagram is not intended to convey the actual circuit implementation, but rather to describe the functionality.)

A single Configurable Logic Block (CLB) contains two function generators, which can be configured as one 16x1 dual-port RAM, as shown in Figure 1, or as a 32x1 single-port RAM. Alternatively,

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the two function generators can be individually configured as any combination of 16x1 single-port RAM and 4-input combinatorial logic functions. The RAM outputs, as with any other function generator outputs, can optionally be registered within the same logic block.

### Edge-Triggered Write

The XC4000E provides the choice of level-sensitive or edge-triggered write capabilities. Both options are available for single-port mode, while dual-port mode is always edge-triggered. Most designers are familiar with level-sensitive RAM. This type of RAM is similar to most SRAM devices available on the market.

One disadvantage of level-sensitive RAM is that it requires a precise timing relationship between the Address, Data and Write Enable signals. Maintaining such relationships inside an array-based device can be difficult because the designer does not have direct control over the routing delays within the device.

A better approach for system design is to use clocked or edge-triggered RAM, because edge-triggered writing simplifies the RAM timing. With the introduction of the XC4000E, this option is now available to FPGA designers. Instead of a complex relationship between various timing parameters, the XC4000E RAM timing operates like writing to a data register. Data and address are presented. The register is enabled, after which a clock edge loads the data into the register as shown in Figure 2.

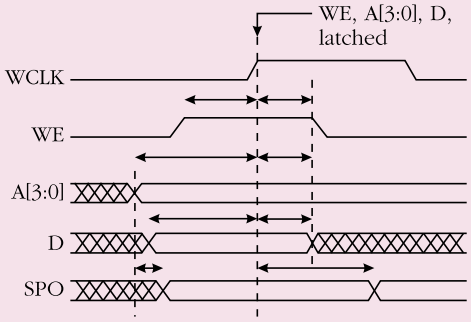


**Figure 2.** *Edge-Triggered RAM Write Cycle*

The signals used during a write operation are described in Table 2. These signals are derived from Figure 1.

During a write operation, data is presented on the D input. The write location is presented on the address inputs, A[3:0]. The RAM block is enabled for writing by a logic high on the write enable input, WE.

The write clock input, WCLK, can be configured as active on either the rising edge (default) or the falling edge. The rising edge will be used throughout these examples. On the rising edge of WCLK, the D, A[3:0], and WE inputs are captured as shown in Figure 2, thereby synchronizing them to the clock.

A short, built-in delay on the WCLK signal allows the signals to propagate through the decoder logic that enables the appropriate memory cell — the one corresponding to the correct address location in the RAM. The data is clocked into the enabled cell by the delayed clock edge. The new RAM data is available at the RAM outputs a short time later. The timing diagram in Figure 2 shows the case where the A[3:0] address does not change, and SPO reflects the data just written.

The WCLK input to the logic block is the same input used to clock the CLB flip-flops, but it can be separately inverted. Consequently, RAM output data can be captured in the flip-flops, if desired, on either the inactive edge or the next active edge of WCLK.

**Table 2.** *Edge-triggered RAM Description*

| Signal | I/O | Description |
|---|---|---|
| A[3:0] | I | Address input for writing both ports of the RAM, and reading the single port. |
| DPRA[3:0] | I | Address input for reading the dual port. |
| D | I | RAM Data input. |
| WE | I | Write enable input. When high, the RAM may be written with the data presented on the D input. |
| WCLK | I | Write clock input. Clocks the data into the RAM when WE is high. Also captures and synchronizes the A[3:0], D, and WE inputs. |
| SPO | O | Single-port RAM output. RAM location is controlled by A[3:0] inputs. SPO is not controlled by the WCLK input. |
| DPO | O | Dual-port RAM output. RAM location is controlled by DPRA[3:0] inputs. DPO is not controlled by the WCLK input. |

### Dual-Port Mode

Most RAMs have a single address port and a single output port. These are called single-port RAMs. However, some applications require more than one port. FIFOs are

one example of an application that benefits from additional output and address ports.

In a FIFO, there are separate read and write addresses for the memory. A FIFO can be implemented using a single-port memory by multiplexing both the read and write addresses onto a single address port. This approach, however, prevents a simultaneous read and write operation. Either a read or a write operation can access the RAM at different times, but not both at the same time. The extra multiplexers and their associated control logic add to the complexity of a RAM-based FIFO design. A dual-port RAM—one with two address inputs and two data outputs—would simplify a FIFO design.

Again, Figure 1 provides an example. The logic in the figure is configured as a 16x1 edge-triggered dual-port RAM. Data can be read and written using the A[3:0] address port and the RAM data appears on the SPO output, just as it would for a single-port RAM.

Simultaneously, data can be read—but not written—using the DPRA[3:0] address port. The RAM data appears on the DPO output. Operations with the DPRA[3:0] address port are independent of the A[3:0] address port. Consequently, a RAM location can be accessed simultaneously through two different ports using the two sets of address and data ports as described in Table 3.

If both addresses point to the same location, and a write is performed using the A[3:0] inputs, data appears first on SPO and then on DPO a short time later.

## Selecting an Appropriate RAM Mode

Table 4 shows the recommended usage for each RAM mode in the XC4000E architecture.

Frankly, there is little reason to use level-sensitive mode in new designs now that edge-triggered RAM is available. In cases where CLB usage must be minimized, single-port edge-triggered mode is recommended. This mode offers the best density, although a lower system throughput than dual-port mode for some applications. If simultaneous read and write capability is an asset and silicon efficiency is not a priority, consider using dual-port, edge-triggered mode for maximum system throughput.

## Schematic Symbols

Using the XC4000E edge-triggered and dual-port RAM capabilities requires special schematic symbols available within the XC4000E library. All edge-triggered RAMs have symbols that begin with “RAM” and end with S (in the case of single-port, edge-triggered RAMs) or D (in the case of dual-port RAMs). If no letter is appended, the level-sensitive RAM is referenced.

## Initializing RAMs

The XC4000E can initialize RAM to a known value during FPGA configuration. All types of XC4000E RAM can be initialized, including the original level-sensitive mode. The INIT attribute or property is used to initialize RAM to a known value. If omitted, the initial value defaults to all zeros. RAM contents are not affected by a global reset.




**Table 3.** *Address Port Functionality*

| Address Port | Operation | Output Data |
|---|---|---|
| A[3:0] | Read and Write | SPO |
| DPRA[3:0] | Read only | DPO |

**Table 4.** *RAM Mode Selection*

| | Level-Sensitive | Edge-Triggered | Dual-Port Edge-Triggered |
|---|---|---|---|
| **Use for New Designs?** | No | Yes | Yes |
| **Density (Registered 16x1)** | 1/2 CLB | 1/2 CLB | 1 CLB |
| **Simultaneous Read/Write?** | No | No | Yes |
| **Relative Performance** | X | 2X | 4X (Effective) |

## Software Support

The edge-triggered and dual-port capabilities are supported in XACT*step*™ version 5.2, or later. An XC4000E update may be required. Edge-triggered, single-port and dual-port RAM are supported in X-BLOX™ with the SYNC_RAM and DP_RAM modules. ◆