worst-case conditions, our devices are tested at a high temperature (85° C junction temperature) and a low supply voltage (4.75 V for 5 V commercial parts).

Estimating Best Case Delays

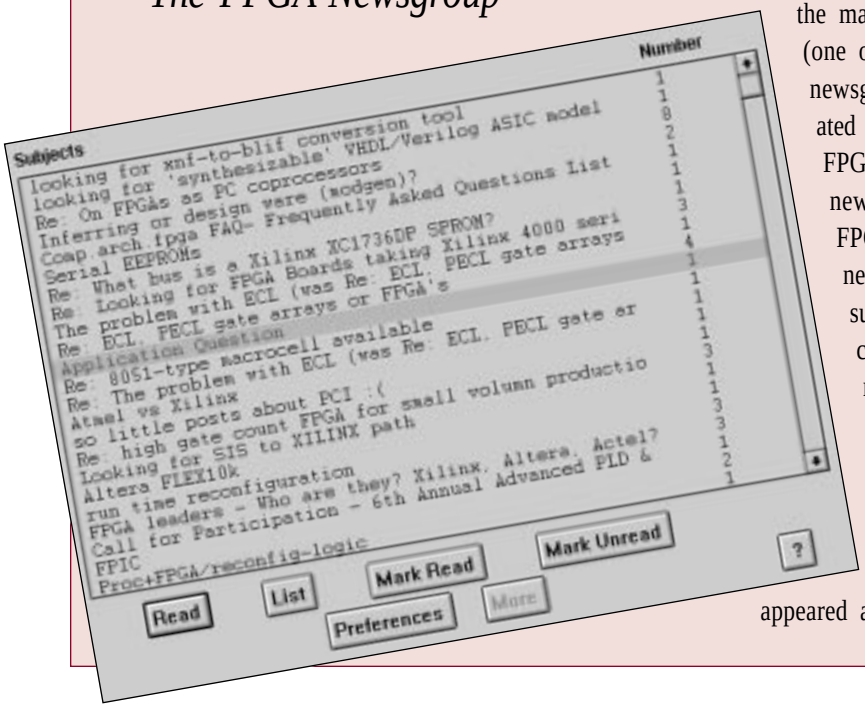
How short can the "best case" delay be when compared to the guaranteed and tested "worst-case" parameters? As an estimate, let's first subtract 10% for tester guardband (devices are always tested to slightly tighter parameters than specified, in order to avoid disagreements over tester calibration. Ten percent is probably very conservative, but 5% would be aggressive.) Then let's subtract 10% for the difference between the 4.75 V test voltage and the 5.25 V best-case supply voltage. Next, we'll subtract 30% for the difference between the 85° C test and the 0° C best-case junction temperature. Finally, we must subtract 40% for the difference between our slowest processing and fastest processing.

Multiplying 0.9 x 0.9 x 0.7 x 0.6 yields 0.34. That means, **you can expect to get a "best-case" delay of about a third of the specified worst-case value** for commercial grade products.

To be very conservative, for any given parameter we suggest that you assume a best-case value of 25% of the worst-case number that we specify for the same parameter *at the fastest available speed grade*. Thus, for the top-of-the-line, fastest part, the ratio between worst- and best-case delay is conservatively estimated as 4:1; for slower parts it is a larger ratio.

However, rather than relying on this estimate, the best advice is to design synchronously, whenever possible, and use devices with non-positive hold time requirements on data inputs. ◆

Visit comp.arch.fpga — The FPGA Newsgroup



Xilinx users with Internet access should review the material in the comp.arch.fpga newsgroup (one of more than 10,000 unmoderated newsgroups on the Internet!). Originally created as a forum for sharing ideas on using FPGAs for new computer architectures, this newsgroup has expanded to discuss all FPGA-related issues. It is a well-mannered newsgroup that covers a wide variety of subjects. Xilinx sometimes "takes it on the chin," as do our competitors, but the newsgroup can be helpful in clarifying confusing issues and tapping into other engineers' experience.

The discussion of minimum timing delays in the article on the page at left is a summation of material that first appeared as a "thread" in this newsgroup. ◆