Trading Off Among the Three Ps

Power, Package & Performance

There are well-defined relationships between chip power consumption, package thermal characteristics, ambient and junction temperature, and device performance.

In many cases, the user has no control over the maximum ambient temperature, but can choose the device and package, and then strive for an acceptable power consumption. In other cases, chip, package, power consumption and ambient temperature are given, and the resulting achievable performance level must be calculated. If performance cannot be sacrificed, thermal management techniques (e.g, airflow and heat sinks) can be used to lower the thermal resistance.

The governing equation is

$$T_J = T_A + P \times \Theta_{J\text{-}A}$$

where T_J = junction temperature

T_A = ambient temperature

$\Theta_{J\text{-}A}$ (Theta J-A) = Thermal resistance of the package-die combination

P = power dissipation

$\Theta_{J\text{-}A}$ is expressed in degrees C of junction temperature rise over the ambient temperature for every Watt dissipated in the device. $\Theta_{J\text{-}A}$ is primarily a function of the package and the airflow, with die size a secondary factor. (Larger die have a lower $\Theta_{J\text{-}A}$ value). *See Table 1.*

When the junction is hotter than 85°C, where Xilinx tests and guarantees performance parameters, delays increase 0.35% for every additional degree C. At 125°C, the maximum allowed junction temperature in a plastic package, delays are 14% longer, and speed is thus 12% lower than the guaranteed values in the data book and the software. In ceramic packages, the maximum allowed junction temperature is 150°C. ◆

Typical thermal resistance for various packages with and without airflow

Package	Still Air	250 ft/min (1.3 m/s)	500 ft/min (2.5 m/s)	750 ft/min (3.8 m/s)	
HQ304	11	7	6	5	°C/W
HQ240	12	9	7	6	°C/W
HQ208	14	10	8	7	°C/W
MQ240	17	12	11	10	°C/W
MQ208	18	14	13	12	°C/W
PQ240	23	17	15	14	°C/W
PQ208	32	23	21	19	°C/W
PQ160	32	24	21	20	°C/W
PQ100	33	29	28	27	°C/W
PC84	33	25	21	17	°C/W
TQ100	31	26	24	23	°C/W
VQ100	38	32	30	29	°C/W

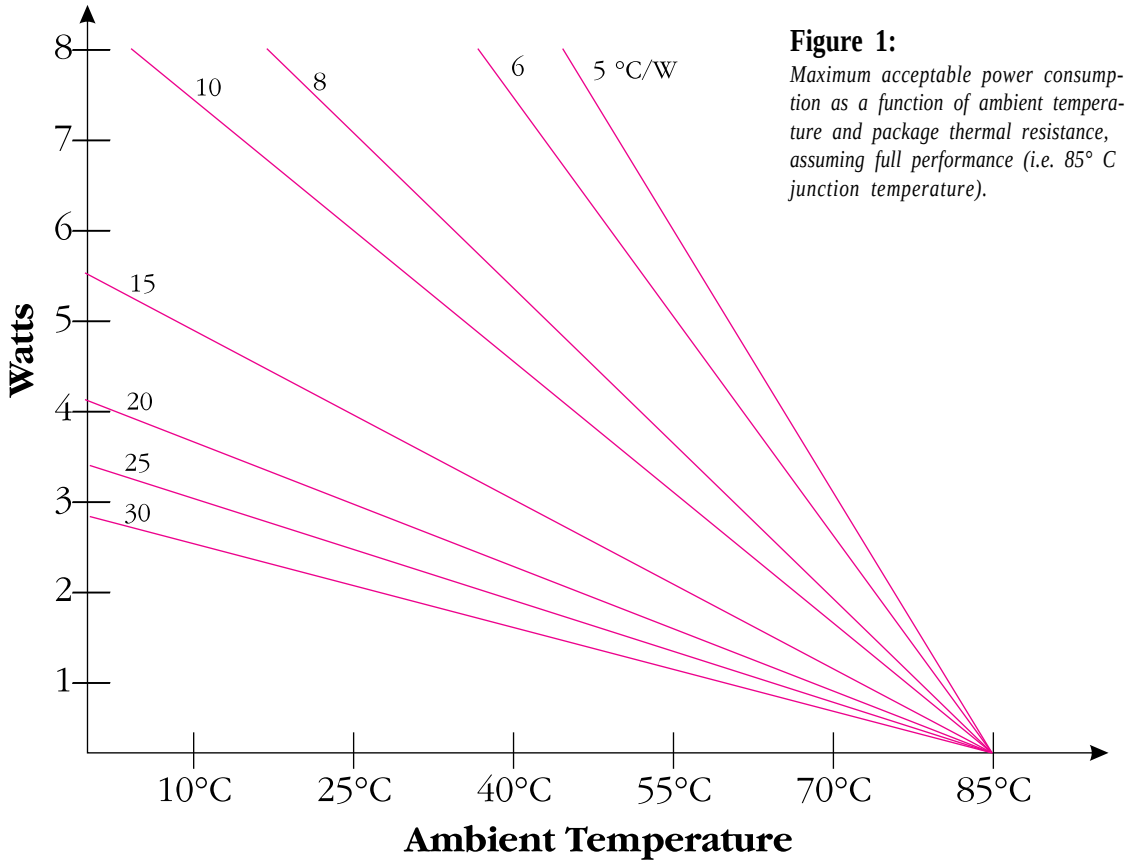

Figure 1:
Maximum acceptable power consumption as a function of ambient temperature and package thermal resistance, assuming full performance (i.e. 85° C junction temperature).

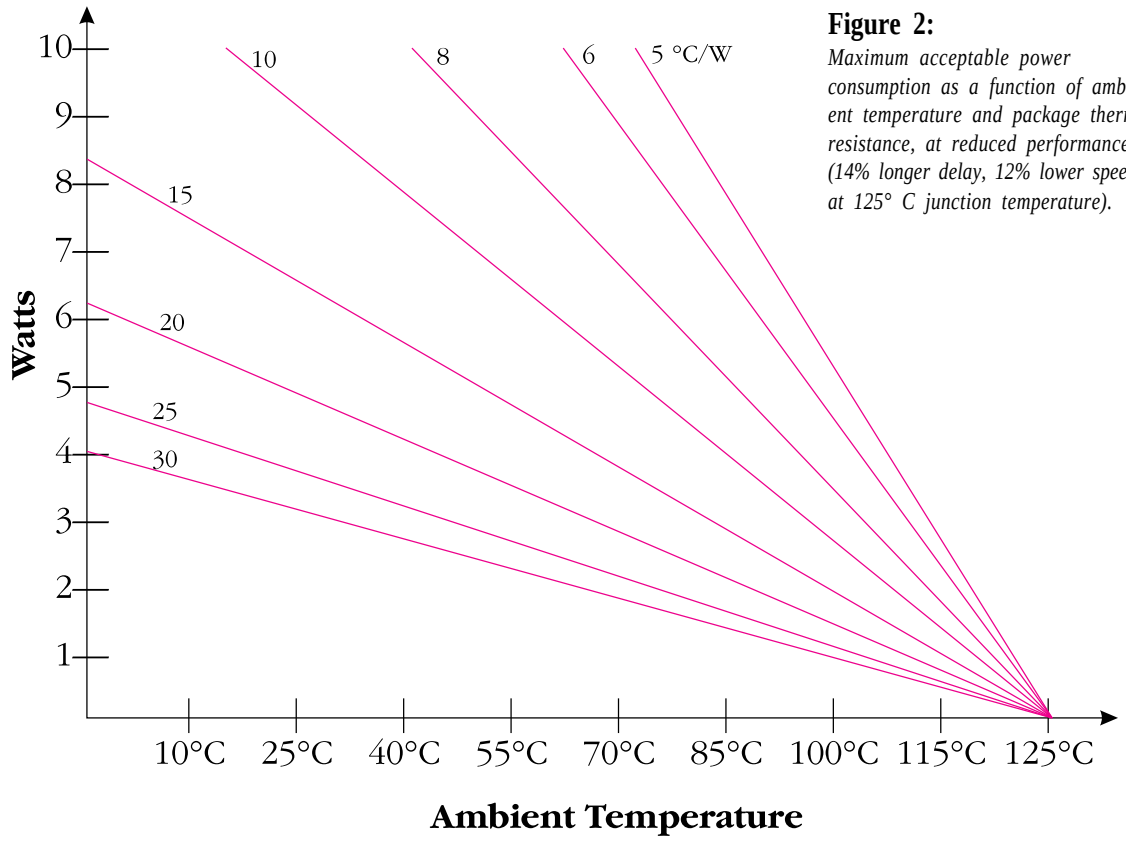

Figure 2:
Maximum acceptable power consumption as a function of ambient temperature and package thermal resistance, at reduced performance (14% longer delay, 12% lower speed at 125° C junction temperature).