CORE Generator for PCI:

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The First Web-Based Development Tool for FPGA Design

This spring, Xilinx introduced an innovative, web-based tool that radically simplifies the use of cores for FPGA design. The new, on-line CORE Generator tool facilitates core usage by enabling designers to instantly access, customize, and download core designs using WebLINX (www.xilinx.com).

It features an intuitive graphical interface, thereby shortening the learning curve for logic designers. Initially designed to support users of the LogiCORE PCI module, the CORE Generator will be extended to support other Xilinx LogiCORE and third-party AllianceCORE products later this year.

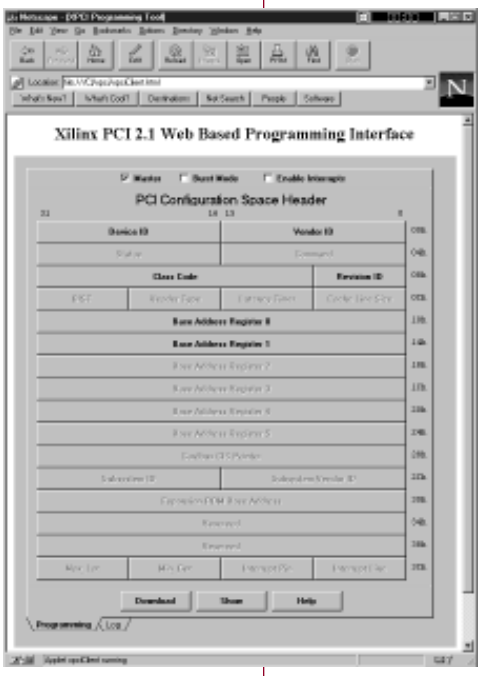

Figure 1: *CORE Generator tool for PCI, main menu*

The CORE Generator tool for PCI introduces a new methodology for acquiring and using cores with FPGAs. Since the tool executes on the web, LogiCORE PCI users always have access to the latest versions of the cores (as well as the latest product information). "Customized" cores are created by the CORE Generator based on user-defined parameters, allowing designers to easily create and download their unique versions of the core netlist, regardless of the design tools and methodologies used for design entry and simulation.

Using CORE Generator

To create a PCI core netlist using the CORE Generator, designers enter their system's parameters by using the program's graphical user interface (GUI). The GUI mirrors the already-familiar PCI Specification Standard table. For example, the GUI includes a copy of the configuration space header from the PCI specification (**Figure 1**); the user simply enters the parameters by selecting the appropriate values in pre-defined menus. The GUI prevents designers from entering invalid parameters. On-line help is available, as well as application notes describing the complete design flow from core configuration to implementation.

The CORE Generator allows the designer to integrate the LogiCORE PCI module using any chosen tool environment, including VHDL, Verilog, or schematic-based design. (Previously, Viewlogic schematic entry tools were required to modify and customize the design.) The CORE Generator creates all the files needed to integrate the PCI core within the FPGA design and verify the results, including:

1) a netlist with constraints that ensure that timing is met without any manual tuning.
2) a "wrapper" used to instantiate the core in a VHDL, Verilog or schematic-based design.
3) a VHDL/Verilog simulation model for functional verification.

These files are then downloaded over the web to the designer's development platform.

The PCI cores created by the CORE Generator are "firm" cores, with relative placement and timing constraints embedded in the netlist to ensure that the performance of the implemented design meets the requirements of the PCI specification. Thus, PCI timing can be met without any manual tuning of the core, and, as a result, engineering resources can be focused on the system-level design, potentially saving months of development time.

Figure 2 compares typical development times and costs for designing a PCI interface from scratch using a generic, synthesizable core and using a proven LogiCORE PCI core.

Visit the VIP Lounge

To access the tool, use a Java-enabled web browser such as Netscape 3.0 or Microsoft Explorer 3.0 to visit WebLINX (www.xilinx.com). The CORE Generator is part of the new "LogiCORE VIP lounge" site that holds useful

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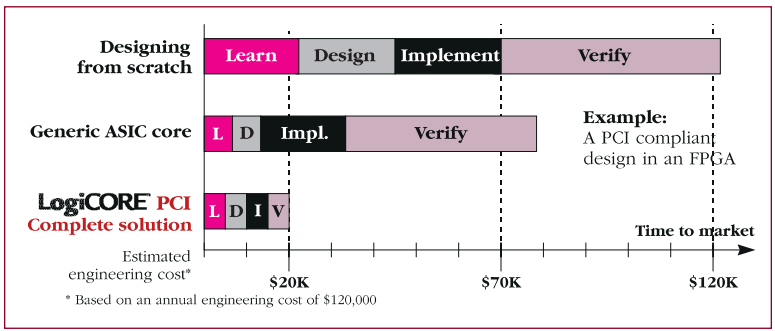
Figure 2: *Proven LogiCORE PCI core cut development time*



information and design files for registered LogiCORE product owners; all users with a valid maintenance agreement can log onto the new LogiCORE lounges and register for access to the CORE Generator. The CORE Generator tool is password protected so that only LogiCORE PCI owners have access to the core.

For now, even WebLINX visitors without a valid maintenance agreement can access a *demonstration* version of the PCI CORE Generator, allowing the evaluation of the GUI and an examination of the various options available for the PCI interface core. In the future, all visitors will be allowed to create functional simulation models for LogiCORE PCI designs, allowing users to create and download the model, instantiate it into a custom design, and perform complete system functional verification, all prior to purchasing the core.

Further information, including the demonstration version of the CORE Generator, can be found at www.xilinx.com/products/logicore/logicore.htm. ◆